

## COMP 222 Spring 2016 Midterm #1 Solutions

Average = 83, Median = 87

Range	# of Papers
100	2
90s	13
80s	8
70s	3
60s	4
<60	3

### P1 Number Systems

A Convert  $EFC2_{16}$  to octal

$$EFC2_{16} = 1110\ 1111\ 1100\ 0010_2 = (1)(110)(111)(111)(000)(010) = 167702_8$$

B Without completing the conversion, show how to express the conversion of  $EFC2_{16}$  to base 10 as a series of terms with coefficients and powers of 16.

$$EFC2_{16} = 14 \times 16^3 + 15 \times 16^2 + 12 \times 16^1 + 2 \times 16^0$$

C Without completing the conversion, show how to express the conversion of  $11110000111100_2$  to base 10 as a series of powers of 2. First show the “obvious” series based on the 1 positions in the number.

$$11110000111100_2 = 2^{13} + 2^{12} + 2^{11} + 2^{10} + 2^5 + 2^4 + 2^3 + 2^2 (= 15420)$$

D Now show the shortcut series based on transitions from 0  $\rightarrow$  1 and 1  $\rightarrow$  0 reading the bits from right to left.

$$11110000111100_2 = -2^2 + 2^6 - 2^{10} + 2^{14} (= -4 + 64 - 1024 + 16384 = 15420)$$

E Look at the following series of calculations. Explain what the calculation is and indicate the final result. Assume all numbers are base 10 and that the calculations are correct.

$3562 \div 8 = 2$	$3562 \div 8 = 445$
$445 \div 8 = 5$	$445 \div 8 = 55$
$55 \div 8 = 7$	$55 \div 8 = 6$
$6 \div 8 = 6$	$6 \div 8 = 0$

*This calculation converts 3562 from base 10 to base 8 octal. Digits are produced right to left, so the final answer is 6752.*

## **P2 Instructions and Languages**

**A** The instruction execution cycle is named after what famous mathematician/computer scientist?

***John von Neuman***

**B** A traditional compiler (e.g. C compiler) translates between what two kinds of language?

***HLL (high level language) to machine language***

**C** The Java compiler is a hybrid compiler because it produces a different kind of output. What?

***JVM bytecodes***

**D** What does the name of the PC register in the CPU stand for and what is its purpose?

***PC = program counter, it holds the memory address of the next instr to be fetched***

**E** Ignoring swap space and cache for now, in the simplest model of program execution, when an instruction is “fetched,” what does that mean? Where is it moved from and moved to?

***From main memory (RAM) to CPU register***

**F** When an application is launched, what is the name of the disk region where the process image is initially created and stored?

***Swap space or page file***

**G** What limitation on process execution would be imposed on a computer system if it did not provide virtual memory?

***Process image would have to completely fit within available RAM at the same time in order to be executed.***

### P3 Cache Associativity

A What is the principle of execution locality?

*Instructions tend to be fetched and executed sequentially from a small subset of memory, not skipping around randomly across the entire memory*

B What is the difference between split and unified cache?

*Split cache: instructions and data are stored in different caches*

*Unified cache: instructions and data are stored in the same cache*

C Imagine a computer system with the following characteristics:

- Installed RAM: 16 GB (gigabytes)
- Total cache capacity: 2 MB (megabytes)
- Size of a cache line: 64 B (bytes)
- Cache associativity: 8 way set associative

Answer the following questions about this computer system:

- How many address bits are required to address each byte location in RAM?  $16\text{ GB} = 2^{34}$ , so 34 bits
- How many lines or blocks in RAM?  $2^{34}/2^6 = 2^{28}$
- How many lines in cache?  $2^{21}/2^6 = 2^{15}$
- How many sets in cache?  $2^{15}\text{ lines} / 2^3\text{ lines per set} = 2^{12}\text{ sets}$
- How many lines per set in cache?  $2^3 = 8$
- Show how to divide an address into tag, set, and byte offset. 16 bits tag | 12 bits set | 6 bits byte offset

**For P4 and P5, only answer one and skip the other.**

**P4** Combinational vs Sequential Circuits, DRAM, SR latch

**A** Briefly explain the difference between combinational and sequential circuits.

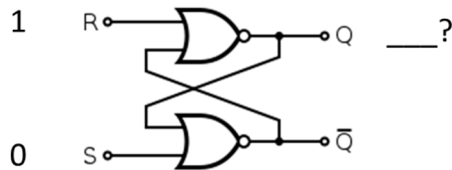
*Combinational Circuit: output is purely a function of input*

*Sequential Circuit: output is a function of both input and previous state*

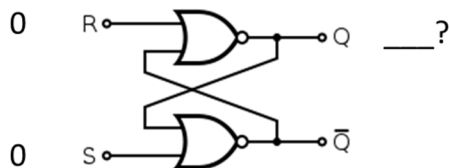
**B** If a DRAM chip is advertised as 2048 X 2048 X 16 with 4 banks, what is its total capacity in bits?

$$2^{11} \times 2^{11} \times 2^4 \times 2^2 = 2^{28} = 256 \text{ Mb (megabit)}$$

**C** The SR latch is a simple model of how static RAM (SRAM) implements storage for a single bit. In the following diagram, for the indicated inputs, show the output implied at Q.



**Q = 0**, bringing the R input high is called the “reset” operation, which sets Q to 0



**Q = 0 or 1**, when both R and S are low, Q retains its previously stored value, which could have been either 0 or 1

For P4 and P5, only answer one and skip the other.

## P5 ECC

**A** Given the 12 bit Hamming SEC code word  $232_{16}$ , extract the 8 bit data word, correcting any single bit error if present.

### Hints

- Number all bits starting at 1 on the right.
- In a 12-bit code word, check bits in positions 1, 2, 4, and 8, and data in positions 3, 5, 6, 7, 9, 10, 11, 12.
  - Check bit 1: data bits 12457
  - Check bit 2: data bits 13467
  - Check bit 3: data bits 2348
  - Check bit 4: data bits 5678

### Steps

- Expanded code word (12 bits, 3 hex): `_0010 0011 0010_____`
- Extracted data word (8 bits): `_0010 .011 .0.. = 0010 0110 = 26_____`
- Extracted check bits (4 bits): `_.... 0... 0.10 = 0010_____`
- Recalculated check bits (4 bits):
 

$$\begin{array}{l} 1: 01000 = 1 \\ 2: 01010 = 0 \\ 3: 1100 = 0 \\ 4: 0100 = 1 \end{array}$$

$$= 1001$$
- Code word bit in error (position):
 

$$\begin{array}{l} 0010 \text{ XOR} \\ 1001 = \\ 1011 = 11 \text{ (codeword bit position)} \end{array}$$
- Data bit in error (position and value): `_code bit 11 = data bit 7, value = 0_`
- Corrected data word (8 bits, 2 hex): `0010 0110 = 0110 0110 = 66`

**B** Using the relationship  $2^k - 1 \geq n + k$ , where  $n$ =number of data bits and  $k$ =number of check bits, determine the minimum number of check bits required for the SEC Hamming code for 64 data bits.

$n$	$k$	$n+k$	$2^k - 1$	<i>Sufficient?</i>
64	5	69	31	$31 \geq 69$ ? No
64	6	70	63	$63 \geq 70$ ? No
64	7	71	127	$127 \geq 71$ ? Yes

*Minimum number of check bits = 7*