COMP 222 Spring 2016 Midterm #1 NAME_____
75 minutes, 4 equally weighted problems each with multiple parts, write answers on this sheet, closed notes.

P1 Number Systems

A Convert $EFC2_{16}$ to octal

B Without completing the conversion, show how to express the conversion of $EFC2_{16}$ to base 10 as a series of terms with coefficients and powers of 16.

C Without completing the conversion, show how to express the conversion of 11110000111100_2 to base 10 as a series of powers of 2. First show the "obvious" series based on the 1 positions in the number.

D Now show the shortcut series based on transitions from 0 ➔ 1 and 1 ➔ 0 reading the bits from right to left.

E Look at the following series of calculations. Explain what the calculation is and indicate the final result. Assume all numbers are base 10 and that the calculations are correct.

```
3562 % 8 = 2      3562 / 8 = 445
 445 % 8 = 5       445 / 8 =  55
  55 % 8 = 7        55 / 8 =   6
   6 % 8 = 6         6 / 8 =   0
```

P2 Instructions and Languages

A The instruction execution cycle is named after what famous mathematician/computer scientist?

B A traditional compiler (e.g. C compiler) translates between what two kinds of language?

C The Java compiler is a hybrid compiler because it produces a different kind of output. What?

D What does the name of the PC register in the CPU stand for and what is its purpose?

E Ignoring swap space and cache for now, in the simplest model of program execution, when an instruction is "fetched," what does that mean? Where is it moved from and moved to?

F When an application is launched, what is the name of the disk region where the process image is initially created and stored?

G What limitation on process execution would be imposed on a computer system if it did not provide virtual memory?

P3 Cache Associativity

A What is the principle of execution locality?

B What is the difference between split and unified cache?

C Imagine a computer system with the following characteristics:

- Installed RAM: 16 GB (gigabytes)
- Total cache capacity: 2 MB (megabytes)
- Size of a cache line: 64 B (bytes)
- Cache associativity: 8 way set associative

Answer the following questions about this computer system:

- How many address bits are required to address each byte location in RAM? _____
- How many lines or blocks in RAM? _____
- How many lines in cache? _____
- How many sets in cache? _____
- How many lines per set in cache? _____
- Show how to divide an address into tag, set, and byte offset. _____

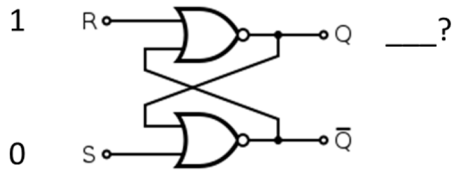
For P4 and P5, only answer one and skip the other.

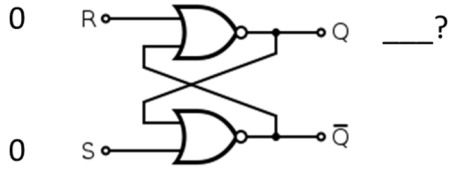
P4 Combinational vs Sequential Circuits, DRAM, SR latch

A Briefly explain the difference between combinational and sequential circuits.

B If a DRAM chip is advertised as 2048 X 2048 X 16 with 4 banks, what is its total capacity in bits?

C The SR latch is a simple model of how static RAM (SRAM) implements storage for a single bit. In the following diagram, for the indicated inputs, show the output implied at Q.





For P4 and P5, only answer one and skip the other.

P5 ECC

A Given the 12 bit Hamming SEC code word $\mathbf{232_{16}}$, extract the 8 bit data word, correcting any single bit error if present.

Hints

- Number all bits starting at 1 on the right.
- In a 12-bit code word, check bits in positions 1, 2, 4, and 8, and data in positions 3, 5, 6, 7, 9, 10, 11, 12.
    - Check bit 1: data bits 12457
    - Check bit 2: data bits 13467
    - Check bit 3: data bits 2348
    - Check bit 4: data bits 5678

Steps

- Expanded code word (12 bits, 3 hex): _____
- Extracted data word (8 bits): _____
- Extracted check bits (4 bits): _____
- Recalculated check bits (4 bits): _____
- Code word bit in error (position*): _____
- Data bit in error (position and value): _____
- Corrected data word (8 bits, 2 hex): _____

*Error position is calculated as a code word position, you must translate it to the corresponding data word position.

B Using the relationship $2^k - 1 >= n + k$, where n=number of data bits and k=number of check bits, determine the minimum number of check bits required for the SEC Hamming code for 64 data bits.