Computer Organization

1. History

Zero\textsuperscript{th} Generation – Mechanical Computation (1642-1945)

- Blaise Pascal calculator [+,-] 1642
- Wilhelm von Leibniz calculator [+,-,\times,\div] \approx 1670 – 1680
- Charles Babbage
  - difference engine [+,-] = 1820 – 1830
  - naval navigation tables
  - single algorithm – finite differences using polynomials
  - analytical engine [+,-,\times,\div]
    - memory (store)
    - computation unit (mill)
    - input unit (punched card reader)
    - output section (card punch & printer)
- Konrad Zuse electromagnetic relays 1930 – 1944
- John Atanasoff Iowa State University
  - binary number system
  - electromagnetic relays
  - memory capacitors
  - differential equations
- George Stibitz Bell Labs
- Howard Aiken MIT 1944
  - Mark I based on Babbage’s analytical engine design
  - electromagnetic relays

First Generation – Vacuum Tubes (1945-1955)

- ENIGMA encryption machine – mechanical device – Germany
- COLOSSUS – vacuum tubes – Alan Turing – Great Britain -- 1943
  - world’s first electronic digital computer
  - logic machine
  - encryption machine
  - Eckert & Mauchley University of Pennsylvania
  - 18,000 vacuum tubes
  - 1500 relays
  - artillery range tables – US Army
  - programming
    - connect sockets with jumper cables
    - set 6000 multi-position switches
• EDSAC – Cambridge University, Great Britain -- Maurice Wilkes 1949

• JOHNIAC Rand Corporation
• ILLIAC University Illinois
• MANIAC Los Alamos Laboratory
• WEIZAC Weizac Institute, Israel

• EDVAC – Electronic Discrete Variable Automatic Computer
  o J. Presper Eckert
  o John Mauchley

• Eckert-Mauchley Computer Corporation
  o Remington-Rand
  o Sperry-Rand
  o Sperry-Univac
  o Unisys

• Honeywell Company of Minneapolis vs. Sperry Rand Corporation
  o Legal Decision over the "ENIAC PATENTS" invalidated the patents on the ENIAC held by the Sperry Rand Corporation because the basic ENIAC ideas of J. Presper Eckert and John Mauchly were "derived from John Atanasoff’s prior work
  o The decision freed the computer industry from the constraints of obtaining license agreements from Sperry-Rand and its descendants

• von Neumann machine – design
  o stored program concept
  o parallel binary arithmetic

• IAS -- Institute of Advanced Studies -- Princeton University
  Herman Goldstine & John von Neumann
  o von Neumann design
  o memory
  o ALR
    • accumulator
  o control unit
  o input
  o output
• Whirlwind I – MIT
  o real-time control
  o magnetic core memory – Jay Forrester

• UNIVAC I – 1951 first commercial computer sold to General Electric
• IBM 701 -- 1953
• IBM 704 – 1956
  o scientific computer
  o 4K core memory
  o 36 bit instructions
  o floating point hardware
• IBM 709 – 1958
  o scientific computer
  o last vacuum tube machine
Second Generation – Transistors (1955-1965)

- transistor -- Bell Labs 1948
  - John Bardeen
  - Walter Brattain
  - William Shockley
  - 1956 Nobel Prize – Physics

- **TX-0** Transistorized eXperimental computer 0
  - MIT Lincoln Laboratory

- Digital Equipment Corporation 1957
  - Kenneth Olson  MIT engineer -- design similar to TX-0
  - PDP-1 1961
  - visual display – screen
  - MIT students -- video games
  - PDP-8 bus architecture

- IBM 7090 – transistorized version of 709
- IBM 7094 – last of the ENIAC type machines
  - parallel binary arithmetic
  - 36 bit registers

- IBM 1401 – business machine
  - no registers
  - serial decimal arithmetic
  - fast I/O
  - byte – 6 bit character, administrative bit, end-of-word bit
  - variable length words

- Control Data Corporation – US Navy
  - William Norris
  - Seymour Cray
  - CDC 6600 1964
    - parallel processing -- multiple functional units
      - addition
      - multiplication
      - division
    - central CPU – number crunching
      - 10 peripheral CPU’s – job control, I/O, etc
  - CDC 7600
  - Cray-1

- Burroughs B5000
  - native language – Algol 60
  - stack architecture

silicon integrated circuit – Robert Noyce 1958

• IBM System/360 Family
  o integrated circuits
  o single assembly language for family
  o 360 Model 30 – accounting machine
  o 360 Model 75 – scientific machine
  o multiprogramming – multiple programs in memory
  o microprogrammed
    ▪ 360 instruction set
    ▪ 1401 instruction set
    ▪ 7094 instructions set
  o emulation of IBM 1401, IBM 7094
  o 16 32-bit registers – binary arithmetic
  o word-oriented registers
  o byte-oriented memory
  o instructions move variable-sized records in memory
  o 16MB address space

• IBM System/370 Family
• IBM System/4300 Family
• IBM System/3080 Family
• IBM System/3090 Family

• CDC PDP-11 Series
  o 16-bit system
  o word-oriented registers
  o byte-oriented memory
  o little brother to IBM 360 series

Fourth Generation – Very Large Scale Integration (1980-?)

VLSI -- Very Large Scale Integration
personal computers
• Intel 8080 chip    CP/M Operating System – Gary Kildall
• IBM Personal Computer – Phillip Estridge – 1981
  o published complete plans – circuit diagrams
  o MS-DOS
  o OS/2 graphical user interface
  o IBM – Microsoft divorce

• Clone Market
• RISC Architecture
• Superscalar Architectures
Moore’s Law empirical observation

- Gordon Moore Intel 1965
- new generation memory chips – every 3 years
- new generation memory size = 4 * old generation memory size
- number transistors per chip doubles every 18 months

Richard Hamming Bell Labs

- $\Delta \uparrow$ quantity $\times 10 \Rightarrow \Delta \uparrow$ quality
  - $\Delta \uparrow$ computer power, constant price
  - $\Delta \downarrow$ price, constant computer power

disposable computers – greeting cards
embedded computers – control systems

- personal computers – workstations
- workstation network – workstation cluster
  mini-supercomputers
- mainframes
  - speed = powerful servers
  - vast disk farms
  - mainframe I/O capacity $\gg$ server system I/O capacity
- supercomputers
  - enormously fast CPU’s
  - huge memory
  - very fast disk drives
  - highly parallel machines

Pentium II

- Intel Corporation 1968 – memory chips
  - Robert Noyce – silicon integrated circuit
  - Gordon Moore
  - Arthur Rock – venture capitalist
- Ted Hoff – placed CPU on a chip
  - Intel 4004 CPU Chip – 1970
  - Intel 8080 CPU Chip – 1974
  - Intel 8086 CPU Chip – 1978
  - Intel 8088 CPU Chip
  - Intel 80286 CPU Chip
  - Intel 80386 CPU Chip
  - Intel 80486 CPU Chip
  - Pentium II
  - 16-bit CPU, 16-bit bus, 1MB limit
  - 16-bit CPU, 8-bit bus, 1MB limit
  - 16-bit CPU, 16-bit bus
  - 32-bit CPU, 32-bit bus
  - 32-bit CPU, 32-bit bus,
  - 8Kb cache memory,
  - floating point unit,
  - multiprocessor support,
### UltraSPARC II

**Sun Microsystems 1982**
- Andy Bechtolsheim
  - SUN-1 Stanford University Network
  - Motorola 68020 CPU
- Vinod Khosla
- Scott McNealy
- Bill Joy
- Sun-1, Sun-2, Sun-3 Workstations
  - Ethernet Connection
  - TCP/IP Software -- ARPANET
- Sun-4 Workstation -- SPARC – Scalable Processor ARCHitecture
  - MicroSPARC
  - HyperSPARC
  - SuperSPARC
  - TurboSPARC
- **UltraSPARC I** 64-bit registers, 64-bit addresses 1995
  - VIS Visual instruction Set
  - images, video, multimedia
- **UltraSPARC II**
- **UltraSPARC III**
picoJava II

Java
- JVM – Java Virtual Machine – internet secure
- object-oriented
- java compiler: Java source code ➔ JVM bytecode
- JVM interpreter: JVM bytecode ➔ executable code

browsers
- JVM interpreter
- JVM JIT Compiler – Just In Time
target machine compiles JVM bytecode
- hardware JVM chips – directly execute JVM binary code
  - JVM interpreter not required
  - JIT Compiler not required
  - embedded systems
  - dynamic modification of functionality
  - Sun microJava 701

Alternative Architectures

- CISC architecture implemented with superscalar technology
- RISC architecture implemented with superscalar technology
- dedicated Java chip for use in embedded systems
2. Computer Systems Organization

Processors, i.e., CPUs

- Control Unit
- ALU
- Register Set
- Internal Buses

von Neumann CPU architecture

Data path cycle process

- access two operands in registers
- insert them into the ALU
- store result in register set

register-memory instructions

register-register instructions
Basic Machine Cycle -- von Neumann

- fetch next instruction from memory; place into IR
- increment PC
- determine instruction type
- if instruction references memory operands, determine memory location
- if necessary, fetch operands into CPU registers
- execute instruction

Interpreter

program that
- runs on a particular machine hardware A, and
- implements the Basic Machine Cycle for a given language L, i.e., L is executed on machine hardware A

Implementation

- specify machine language L for computer design A
- construct hardware processor A to execute instructions, or
- write interpreter for language L that runs on machine hardware B

If the machine hardware B with the native language $L_B$ has a large instruction set with many complicated instructions and if the machine hardware A and its native language $L_A$ has a simple instruction set then it may be less expensive to write an interpreter for the language $L_B$ that would run on the machine hardware A than to actually construct the hardware for B; the trade-off is that the language $L_B$ using the interpreter to execute on machine A will not execute as fast as the same language $L_B$ executing directly on hardware for B

CISC – Complex Instruction Set Computer

complex instructions ➔ faster program execution
- fewer fetch cycles
- overlapped or parallel execution on different hardware
thus high performance systems accumulated many complex instructions
IBM Family Architecture

- many different types of machines with different capabilities
- maintain a single language $L$ across all the different machines
- implement the language $L$ using different implementation strategies on different machines, i.e., interpretation
- one architecture

one architecture across many diverse hardware platforms

low cost systems
- cost outweighs performance
- semiconductor chip technology
- interpreter based design

DEC VAX
- $\approx 600$ instructions $\Rightarrow$ large number of marginal instructions
- 200 ways to specify operands
- all machines used interpretation; no direct execution
- no high-performance model

Motorola 68000
- large interpreted instruction set

control store
- fast read-only memories
- hold interpreter

microinstruction
- interpreter instruction

RISC
- Reduced Instruction Set Computers
- direct execution of instruction set
- backward compatibility not required – new instruction set possible
- instruction set selected that would maximize performance
- instructions with high issue rate -- that could be started quickly

main memory speed $\approx$ read-only control store memory speeds
RISC DEC Alpha

CISC Intel Pentium

- Intel 486 CPU contains RISC core
  - executes simple instructions in a single data path -- RISC
  - interprets complex instructions -- CISC
- backward compatibility – software market

Design Principles

- common instructions are executed directly on the hardware
- complex instructions, rarely used, may be interpreted
- maximize rate of instruction issuance
  - instructions are encountered in program order
  - instructions are not always issued in program order
  - instructions need not finish in program order
- instructions should be easy to decode
  - determine required resources
  - fixed length, regular, small number of fields
- limit memory references to LOAD & STORE instructions
- require operands of most instructions to come from registers
- provide many registers – minimize memory references
Instruction Level Parallelism

- IBM Stretch Computer
- fetch instructions from memory in advance
- store them in a set of registers – prefetch buffer

Pipelining

- divide instruction execution into stages
- each stage of execution is handled by a dedicated hardware unit
  - instruction fetch unit
  - instruction decode unit
  - operand fetch unit
  - instruction execution unit
  - write back unit
- latency vs. processor bandwidth trade-off

```
cycle time of T nanosec &
n stage pipeline ➔
latency of nT nanosec &
bandwidth of 1000/T MIPS
```

Superscalar Architecture

Dual Pipeline Architecture

- instruction fetch unit
- fetches pairs of instructions

instructions must not have resource conflicts
hardware detection & elimination of conflicts
Intel 486
- one pipeline

Pentium
- two pipelines (five-stage)
  - u pipeline -- primary pipeline
    - execute arbitrary instruction]
  - v pipeline – secondary pipeline
    - execute simple integer instructions
  - instructions were always executed in order

Single Pipeline with Multiple Functional Units

transmission rates
copper wire – optical fiber
20 cm/nanosecond

instruction level parallelism
execution speed improvement – maximum
five fold ➔ ten fold
Processor Level Parallelism

**Array Computer**
- single control unit
- large number of identical processors
- different data sets assigned to different processors
- each processor performs the same sequence of instructions on its respective data set

**Vector Processor**
- single control unit
- vector register
  - single instruction loads vector from memory
  - single instruction saves vector to memory

  vector 1
  - v12
  - v11

  vector 2
  - v22
  - v21

  ADDER Unit
  - v12+v22
  - v11+v21
  - result vector

  - executes instruction on sequential pairs of data elements
  - vector processor can be incorporated into conventional processor

**Multiprocessors**
- multiple CPUs sharing common memory
- memory bus contention

**Multicomputers**
- multiple computers, i.e., CPUs with independent memory
- message passing between computers
Memory

bit -- storage location 0/1
byte -- 8 bits
word -- n bytes

BCD addresses
• m bits $\leftrightarrow$ maximum number of directly addressable cells $= 2^m$
• n cells $\leftrightarrow$ addresses range from 0 to n-1
• cell contains k bits $\leftrightarrow 2^k$ different bit combinations $\leftrightarrow 2^k$ different values represented

address length
• determines maximum number of directly addressable cells in memory
• number of bits per cell is independent of address length

Byte Ordering

bytes in a word can be numbered from
• left to right 1 2 3 4 5 6 7 8 $\leftrightarrow$ big endian system
or
• right to left 8 7 6 5 4 3 2 1 $\leftrightarrow$ little endian system

Error Correcting Codes

n-bit codeword
• m-bit word
• r-check bits (redundant information)

Hamming Distance
• number of differing bits between two words
  o compute exclusive or
  o count number of bits that equal 1 in the result

Two words with Hamming distance d between them
$\leftrightarrow$
d single-bit errors must have occurred to convert one into the other

• error-detecting & error-correcting properties depend upon the Hamming distance
• distance d+1 code $\leftrightarrow$ detects d single-bit errors
  o parity bit -- even/odd -- hamming distance 2
Selected Error Correcting Code

- bit 1: leftmost high-order bit
- bit \( n = 2^k \) for some integer \( k \) \( \iff \) parity bit
- bit \( n \neq 2^k \) for any integer \( k \) \( \iff \) data bit

21 bit codeword \( \iff \) 16 bit word + 5 parity bits

bit 1 checks 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21
bit 2 checks 2*1, 2*1+1, 2*3, 2*3+1, 2*5, 2*5+1, 2*7, 2*7+1, 2*9, 2*9+1
bit 4 checks 4*1, 4*1+1, 4*1+2, 4*1+3, 4*3, 4*3+1, 4*3+2, 4*3+3, 4*5, 4*5+1
bit 8 checks 8*1, 8*1+1, 8*1+2, 8*1+3, 8*1+4, 8*1+5, 8*1+6, 8*1+7
bit 16 checks 16*1, 16*1+1, 16*1+2, 16*1+3, 16*1+4, 16*1+5
3. **Peripherals**

**Memory Hierarchy**

<table>
<thead>
<tr>
<th>Media</th>
<th>Speed</th>
<th>Volume</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Registers</td>
<td>nanosec 5-10</td>
<td>128 bytes</td>
</tr>
<tr>
<td>Cache Memory</td>
<td>nanosec 10-50</td>
<td>megabytes 1-5</td>
</tr>
<tr>
<td>Main Memory</td>
<td>nanosec 50-100</td>
<td>megabytes 10-10K</td>
</tr>
<tr>
<td>Magnetic Disk</td>
<td>millisec 10+</td>
<td>gigabytes 2-50</td>
</tr>
<tr>
<td>Tape Storage</td>
<td>seconds</td>
<td>unlimited</td>
</tr>
<tr>
<td>Optical Disk</td>
<td>seconds</td>
<td>unlimited</td>
</tr>
</tbody>
</table>

**Magnetic Disk Storage**

- tracks
- sectors (fixed-length)
  - preamble
  - 512 data bytes
  - ECC Hamming Code; Reed-Solomon Code
  - intersector gap
- cylinders
- zones
  - 10-30 per disk
  - sectors per track depend upon zone

unformatted capacity = preambles + ECC + gaps + formatted capacity

15% total capacity used for
- preambles
- ECC
- intersector gaps

- seek time 5 – 15 millisec
- rotational latency 4 – 8 millisec
- transfer rate 5 – 20 MB/sec

audio-visual disk drives
- do not recalibrate their positioning mechanisms

disk controller (CPU)
- accept O/S commands, e.g., READ, WRITE, FORMAT
- convert 8-bit byte into serial bit stream
IDE Disks

O/S places command parameters in CPU registers
BIOS (Basic Input Output System) \(\rightarrow\) ROM
BIOS issues machine instructions to load disk controller registers
controller specifies head, cylinder, & sector addresses

IDE limits:
- heads 16
- cylinders 63
- sectors 1024

EIDE Disks

LBA (Logical Block Addressing)
- sectors \(2^{24}\)

controller converts
LBA addresses
to
head, sector, & cylinder addresses

SCSI Disks

Unix Workstations
Macintosh Systems
Intel Network Servers

- SCSI Controller
- Bus
- peripheral SCSI Devices (7)
- daisy chain
- terminate last device

concurrent operation
- SCSI controllers
- peripheral SCSI devices

action initiators
- SCSI controllers
- peripheral SCSI devices

action recipients
- SCSI controllers
- peripheral SCSI devices
RAID  Redundant Array of inexpensive Disks
versus
SLED -- Single Large Expensive Disk

parallel I/O operations
Wide SCSI Controller + 15 SCSI Disks

**Raid Level 0**

distribute data across multiple disks
k sectors of virtual disk \(\rightarrow\) strip on actual disk

RAID disks MTF 20,000 hours \(\rightarrow\) RAID failure every 5000 hours
SLED failure every 20,000 hours
operational degradation

**Raid Level 1**
Raidd Level 0 System with Mirrored Backup, i.e., redundancy

write \(\rightarrow\) primary disk & backup disk  speed == SLED
read \(\leftarrow\) primary disk | backup disk  speed == 2X SLED

excellent fault tolerance

**Raid Level 2**

byte (8-bit) \(\rightarrow\) nibble1 + nibble2
nibble1 + 3 parity bits \(\rightarrow\) word (7-bits) : parity bits 1, 2, 4
nibble2 + 3 parity bits \(\rightarrow\) word (7-bits) : parity bits 1, 2, 4
rotationally synchronized drives
distribute one bit per word on each of seven different drives

very high data rate
separate I/O requests per second == SLED
large overhead

The Thinking Machine CM-2
32-bit data words + 6 parity bits \(\rightarrow\) 38-bit Hamming word
38-bit Hamming word + 1 parity bit for resulting word
distributed over 39 disk drives
overhead 19%
Raid Level 3

data word + parity bit
rotationally synchronized drives
distribute one bit per word on each of several different drives
write parity bit on parity bit drive

very high data rate
separate I/O requests per second == SLED

disk crash
“bad” bit position known
assume bit == 0; compute parity
parity error ➔ bit = 1

Raid Level 4
Raid Level 0 System with Parity Disk

parity strip ← ^ (data strip from each data disk)
data change ➔ read n drives, recalculate parity,
write at least two drives
heavy load on parity drive ➔ bottleneck

Raid Level 5
Raid Level 4 System without Parity Disk

distribute parity bit across data disks (round robin)
disk crash ➔ reconstructing drive contents complex process
CD-ROM Storage

potential enormous capacity

Philips LaserVision

Red Book

audio CD
polycarbonate resin + reflective aluminum
low-power laser diode
pits -- height ¼ wavelength of laser light
lands
light reflecting off pit
• ½ wavelength out of phase with light reflecting off land
pit – land transition ➔ 1
land – pit transition ➔ 1
transition absence ➔ 0

continuous spiral
starts at center, progresses to outer edge
rotational rate continuously reduced
varies from 530 to 200 RPM

Magnetic Disks
3600 – 7200 RPM

8-bit byte + 6-bits error code ➔ 14-bit symbol

frame 588-bits
• 24 data byte symbols
• 18 error correction & control symbols

• 192 data bits; 24 data bytes
• 396 error correction & control bits
Yellow Book
CD-ROM's (Compact Disc–Read Only Memory)

8-bit byte + 6-bits error code ➔ 14-bit symbol

frame 588-bits
• 24 data byte symbols
• 18 error correction & control symbols
• 192 data bits; 24 data bytes
• 396 error correction & control bits

CD-ROM sector
98 frames
16-bit preamble
• sector recognition code (12 bytes)
  00 FF FF FF FF FF FF FF FF FF FF FF 00
• sector number (3 bytes)
• mode (1 byte)
  o mode1
    • 16 byte preamble
    • 2048 data bytes
    • 288 byte error correcting code
      cross-interleaved Reed-Solomon code

Error Correction
• within symbol
• within frame
• within CD-ROM sector

98 frames (7203 bytes) ➔ 2048 data bytes
28% efficiency

o mode2
  • 2336 byte data field
  • no error correction
  • audio-video

Green Book
graphics
interleave audio, video, data in same sector
High Sierra File System

Level 1
  • MS-DOS file name convention
  • directory depth limited to 8
  • contiguous files

Level 2
  • file name convention 32 characters

Level 3
  • noncontiguous files

Rock Ridge Extensions
  • Unix naming convention
  • UID’s
  • GID’s
  • symbolic links
CD-Recordable Storage  CD-R

laser guide – 0.6mm groove
gold reflective surface
dye
  • cyanine -- green
  • pthalocyanine -- yellowish orange
  • initial state -- transparent
write (8-16mW)
  • changes molecular structure
  • produces color
read (0.5mW)
  • detects color change

Orange Book
CD-ROM XA -- incremental writing

CD-ROM track
  • group of consecutive sectors written at same time
  • VTOC (Volume Table of Contents)
  • O/S searches for most recent VTOC – current status
  • file deletion
    o file is not listed in most recent VTOC
    o illusion of being deleted
  • session
    o group of tracks

  each track must be written in one contiguous operation without stopping

CD-Rewritables Storage  CD-RW

recording layer -- alloy
  o silver
  o indium
  o antimony
  o tellurium

stable states
  o crystalline high reflectivity
  o amorphous low reflectivity

transitions
  o high power: crystalline state \(\rightarrow\) amorphous state (pit)
  o medium power: reforms crystalline state (land)
  o low power: state can be sensed without state transition
**DVD**

Digital Versatile Disk

CD media
- smaller pits
- tighter spiral
- red laser (supermarket checkout stands)
capacity increase 7X CD-ROM's
capacity 4.7GB
second laser required to read CD-ROMs

formats
<table>
<thead>
<tr>
<th>Format</th>
<th>Capacity</th>
</tr>
</thead>
<tbody>
<tr>
<td>single-sided, single-layer</td>
<td>4.7 GB</td>
</tr>
<tr>
<td>single-sided, dual-layer</td>
<td>8.5 GB</td>
</tr>
<tr>
<td>double-sided, single-layer</td>
<td>9.4 GB</td>
</tr>
<tr>
<td>double-sided, dual-layer</td>
<td>17.0 GB</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Layer</th>
</tr>
</thead>
<tbody>
<tr>
<td>semireflective layer</td>
</tr>
<tr>
<td>reflective layer</td>
</tr>
<tr>
<td>blank substrate layer</td>
</tr>
<tr>
<td>reflective layer</td>
</tr>
<tr>
<td>semireflective layer</td>
</tr>
</tbody>
</table>

consortium of consumer electronics companies computer & telecommunications industries were not invited

intentional incompatibility -- different standards
- US
- Europe
- Asia

video-on-demand ➔ cable systems
**Input/Output**

motherboard
bus (etched into motherboard)
- high speed
- low speed

I/O Device
- controller -- etched into motherboard | board plugged into motherboard
- I/O unit (e.g., disk drive)
- connection cable

ccontroller ↔ device data passed via a serial bit stream

**DMA** Direct Memory Access
- controller accesses memory without CPU intervention
- interrupts upon completion

CPU -- I/O Controller Contention
bus arbiter
preference: I/O devices >> CPU

cycle stealing

ISA Bus -- Industry Standard Architecture Bus

EISA Bus -- Extended ISA Bus

PCI -- Peripheral Component Interconnect Bus

**Keyboard**
- key depressed ➔ interrupt ➔ interrupt handler
  reads hardware register
  obtains key code

- key released ➔ interrupt ➔ interrupt handler
  reads hardware register
  obtains key code

**CRT Monitors** Cathode Ray Tube
- raster scan device
- full screen image -- repainted 30-60 times per second
- grid voltage controls electron flow
- screen glows when hit by electrons
Flat Panel Displays

**LCD**  Liquid Crystal Display  
- viscous organic molecules  
- flow like liquid  
- crystalline spatial structure  
- electrical field changes molecular alignment; i.e., optical properties  
- **NT** -- Twisted Nematic Display  
  - rear plate  
    - horizontal grooves  
    - horizontal polaroid  
  - front plate  
    - vertical grooves  
    - vertical polaroid  
  - light rotates between rear projection plate and front plate  
    - absence of electric field  \(\rightarrow\) screen uniformly bright  
    - voltage applied to selected portions of the plate  
      - twisted structure destroyed  \(\rightarrow\) blocking light  
  - passive matrix display  
  - active matrix display

Character Mapped Terminals

array of characters  
serial communications board -- video board  
video memory  
- [character byte; attribute byte]  
fetch [char; attr] from RAM  
generate analog signal that controls electron beam scanning
Bit Mapped Terminals

array of pixels
supports windows
considerable amount of video RAM

ture color
• 3 bytes per pixel
color palette -- hardware table
• 256 entries -- 24-bit RGB value
• 8 bit index per pixel
RGB -- red, green, blue

performance
• placing data into video RAM uses system bus
• system degradation

RS-232-C Terminals

EIA Standard
UART Universal Asynchronous Receiver Transmitter

parallel to serial conversion
• byte ➞ start bit + data bit stream + stop bit

serial to parallel conversion
• start bit + data bit stream + stop bit ➞ byte
Printers

- matrix printer
- inkjet printers
- laser printers
  - print engine
  - memory x MB
  - CPU
  - Adobe PostScript Language
- halftone -- shades of gray
- color printers
  - CYMK cyan, yellow, magenta, black
  - gamut -- set of colors possible to produce
- ink-jet printers
  - dye-based ink -- fades under ultraviolet light
  - pigment-based ink -- particles clog nozzles
- solid ink printers
  - hot ink reservoirs
  - startup times -- 10 minutes
- color laser printer
  - huge memory requirements
  - stable images
- wax printer
- wide ribbon -- 4 color wax
- costly consumables
- dye sublimation printer
- thermal print head
- dyes vaporized; absorbed onto paper
- nearly continuous colors -- no halftoning required
Modems

- carrier wave -- pure sine wave between 1000 Hz & 2000 Hz
- amplitude modulation -- voltage difference <0,1>
- frequency modulation -- carrier frequency difference <0,1>
- phase modulation -- carrier phase reversal 180 degrees
  when data switches values 0→1 | 1→0
  - dibit phase encoding -- 45°, 135°, 225°, 315°
  - represents 00, 01, 10, 11
- baud rate -- number of potential signal changes per second
- bit rate -- number of bits per second
- start bit + 8-bit byte stream + stop bit
- full duplex -- simultaneous transmissions in both directions
- half-duplex -- transmit in one direction at a time
- simplex -- transmit in one direction only

ISDN Integrated Services Digital Network

- two independent data channels 64KB/second
- signaling channel 16KB/second
- transmission channel multiplexed into 144KB/second
- T interface + NT1 device + U interface

ASCII American Standard Code for Information Interchange

- 7 bit code
- data transmission

UNICODE

- 16 bit code
Digital Logic

kimki
MicroArchitecture Organization

bybvyvg
Operating System Architecture
Assembly Language Process