Pierce College

CSIT 546

Midterm Examination
12 April 2011

Name: ___________________ KEY _______________________

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1.
   a. Describe the **major registers** and other components in the CPU of a von Neumann machine. (10 points)

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<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC</td>
<td>program counter</td>
</tr>
<tr>
<td>IR</td>
<td>instruction register</td>
</tr>
<tr>
<td>MAR</td>
<td>memory address register</td>
</tr>
<tr>
<td>MBR</td>
<td>memory buffer register</td>
</tr>
<tr>
<td>I/O AR</td>
<td>I/O address register</td>
</tr>
<tr>
<td>I/O BR</td>
<td>I/O buffer register</td>
</tr>
<tr>
<td>PSW</td>
<td>Program Status Word</td>
</tr>
</tbody>
</table>

   b. Describe, in detail, the machine cycle of a von Neumann machine including the retrieval of the data items. As part of this description, draw the **Instruction Cycle State Diagram** including **Interrupt Processing**. (15 points)

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   ![Instruction Cycle State Diagram](image)

   c. What is a **Process Control Block (PCB)** and how is it used? (5 points)

   pg 276
   
   data structure containing register contents, open files info, etc used to store process info during transit/wait time in
   - short-term ready queue
   - i/o queues
   - etc
2. For each of the following Cache Memory Systems, describe the advantages & disadvantages of the particular system

a. Direct Mapped Cache System
   i. Advantages
      Easy implementation
      Simple circuitry
      Fast operation
   
   ii. Disadvantages
      Each block maps to only one cache line (inflexible)

b. Associative Mapped Cache System
   i. Advantages
      Blocks map to any cache line
      Less cache misses
   
   ii. Disadvantages
      Complexity of circuitry
      Longer access time – needs to check all tags

c. Set-Associative Mapped Cache System
   i. Advantages
      Can be used as direct mapped cache or associative mapped cache
      Block can be mapped to any line is a set
      Flexible
      Less cache misses
   
   ii. Disadvantages
      More complexity of circuitry than simple associative mapped cache
      Somewhat longer access time – needs to check all tags in the set
      Complicated caching algorithm
3. Limiting the discussion to DRAM and SRAM cells, which one satisfies which criteria: (20 points)

<table>
<thead>
<tr>
<th>Dynamic RAM and Static RAM</th>
</tr>
</thead>
</table>

a. Inexpensive

DRAM

i. Why?

Fewer transistors (1 vs 6)

b. Compact

DRAM

c. Faster

SRAM

d. Digital Device

SRAM

e. Analog Device

DRAM

f. Used to construct Main Memory chips

DRAM

g. Used to construct Cache Memory chips
SRAM

4. Discuss the major differences between SDRAM and DRAM memory.

Dynamic RAM and Synchronous DRAM

(20 points)

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DRAM
Asynchronous using system clock & standard bus with wait states

SDRAM
Synchronous using external clock
running at processor-memory bus speed without wait states
Operations performed on blocks of chips in parallel, i.e., simultaneously