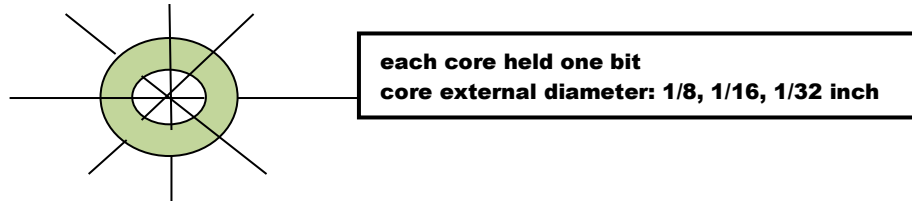


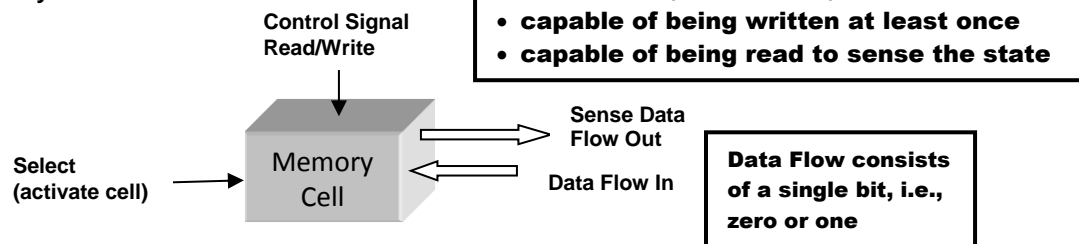
## Internal Memory

### Core Memory



### Semiconductor Memory

- memory cell

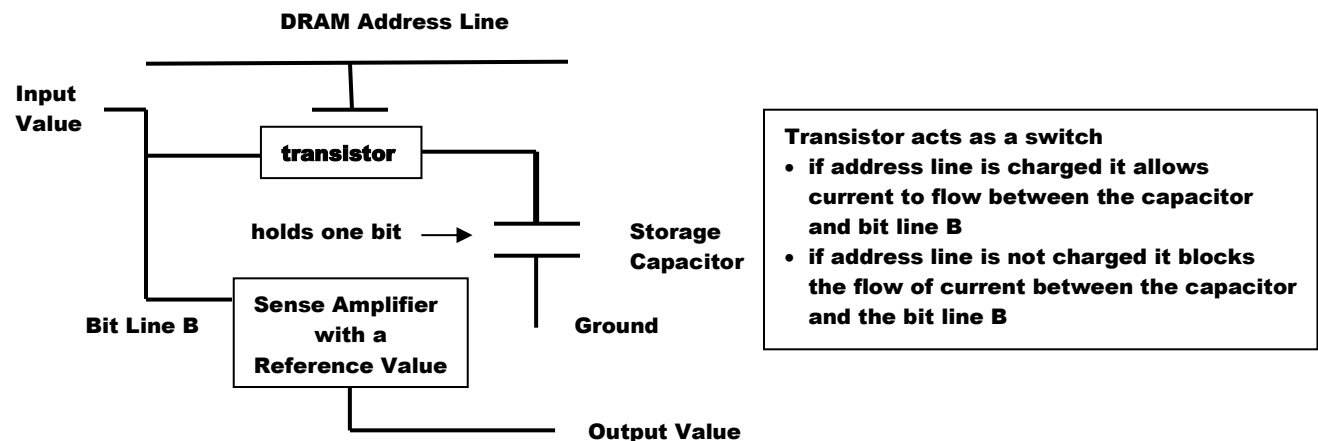


- **RAM Memory**
  - wired-in addressing logic – are used to access individual words
  - rapid reading & writing is possible
  - volatile – constant power supply required
  - temporary storage
- **ROM/PROM Memory – (read only, programmable read-only)**
  - read-only
  - non-volatile
  - permanent storage
- **EPROM Memory (erasable & programmable)**
  - mostly read-only
  - erasable & writable via UV light source (off-line)
  - non-volatile
  - permanent storage
- **EEPROM Memory (electronically erasable & programmable)**
  - mostly read-only
  - electronically erasable & writable (on-line)
  - non-volatile
  - permanent storage
- **Flash Drive Memory**
  - block-level read & write – slow (storage device)
  - mixed features of both main memory & disk storage
  - electronically erasable & writable (on-line)
  - non-volatile
  - permanent storage

## RAM Memory -- used for Main Memory

### DRAM – dynamic RAM

- DRAM cells store a charge on a capacitor
  - presence of a charge indicates 1
  - absence of a charge indicates 0
- capacitors have a natural tendency to discharge → require periodic recharging
- tendency of the stored charge to leak away → ***dynamic***
- analog device, i.e., Sense Amplifier ***measures*** the Storage Capacitors contents



#### Write Operation

1. Voltage signal is applied to the bit line
  - High voltage == 1
  - Low voltage == 0
2. Signal is applied to the address line allowing the charge to be transferred to the capacitor

#### Read Operation

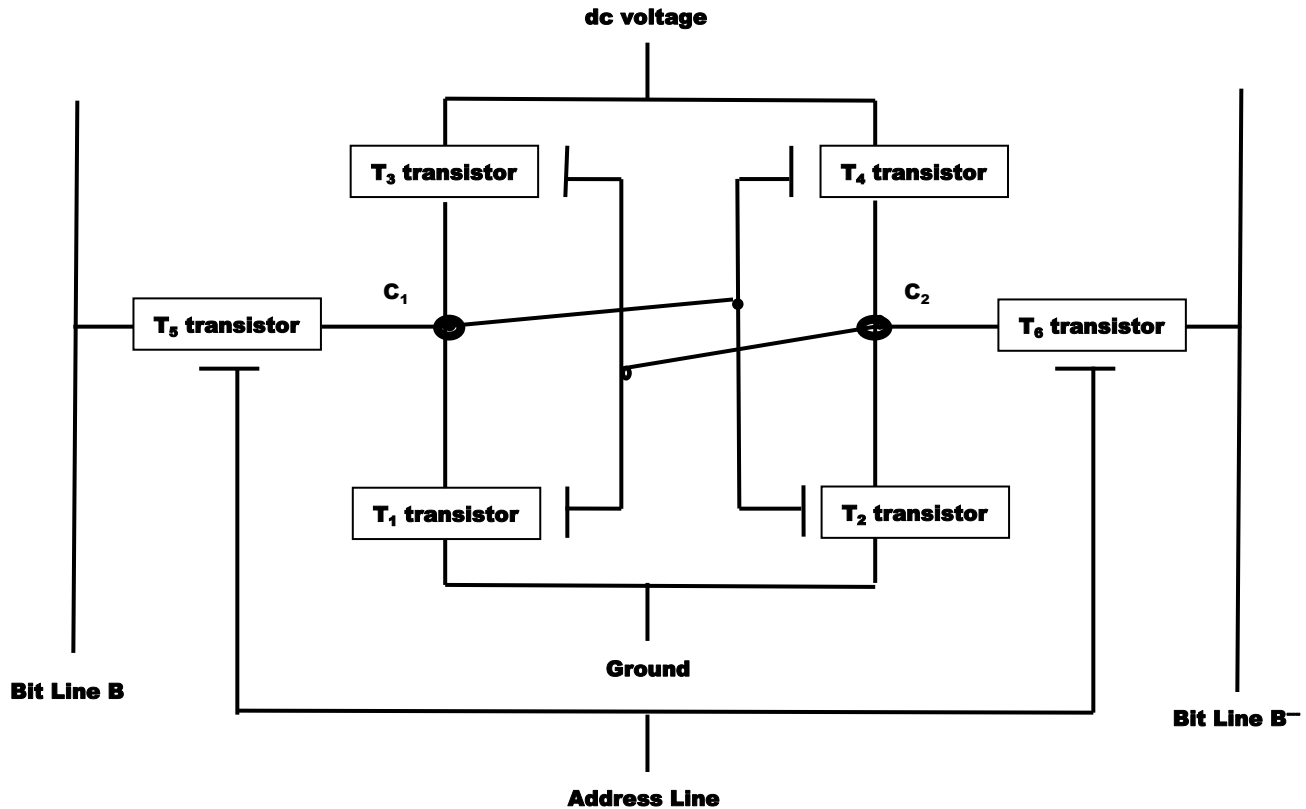
1. Signal is applied to the address line allowing the charge on the capacitor to be released via the bit line to a sense amplifier
2. Sense amplifier compares the capacitor voltage to a reference value and determines whether the cell contains a zero (0) or a one (1)
3. Since the capacitor is now discharged, it must be rewritten to complete the operation

#### DRAM cells are ANALOG DEVICES

since they use a capacitor to hold a voltage charge which must be **MEASURED** to determine whether it represents a zero or a one, i.e., the capacitor may hold any charge value within a specified range

SRAM – static RAM – used for Cache Memory

- digital device
- flip-flop logic-gate
- holds data as long as power supply exists
- no refresh is required to hold data



#### Logic State 1

point C<sub>1</sub> – high } T<sub>1</sub> & T<sub>4</sub> off  
point C<sub>2</sub> – low } T<sub>2</sub> & T<sub>3</sub> on

#### Logic State 0

point C<sub>1</sub> – low } T<sub>1</sub> & T<sub>4</sub> on  
point C<sub>2</sub> – high } T<sub>2</sub> & T<sub>3</sub> off

SRAM address line is used to open/close the transistor switches T<sub>5</sub> & T<sub>6</sub> which allows a read/write operation

#### Write Operation

- desired bit value is supplied to bit line B and the complement value is supplied to bit line B<sup>bar</sup>
- the four transistors T<sub>1</sub>, T<sub>2</sub>, T<sub>3</sub>, T<sub>4</sub> are forced into proper state to hold the desired bit value

#### Read Operation

- bit value is read from bit line B

#### DRAM versus SRAM

- DRAM cells – main memory
  - are simpler & smaller than SRAM cells
  - can be more tightly packed together than SRAM cells
  - inexpensive
  - require refresh circuitry
- SRAM -- cache memory
  - faster than DRAM – do not require rewriting upon reading

## ROM Memory

- data is permanently in main memory, i.e., read-only
- program permanently in main memory
- nonvolatile
- no power source required
- information is “burned”, i.e., “hard-wired” into chip during fabrication
- chip creation must be exact – an error in a single bit invalidates the entire chip run
- high-volume production runs

### Usage:

- microprogramming
- library subroutines
- system programs
- function tables

## PROM Memory – programmable ROM

- data is permanently in main memory, i.e., read-only after write-once
- program permanently in main memory
- nonvolatile
- no power source required
- information is electronically inserted into the chip after fabrication using special equipment while the chip is off-line
- low or medium volume production runs

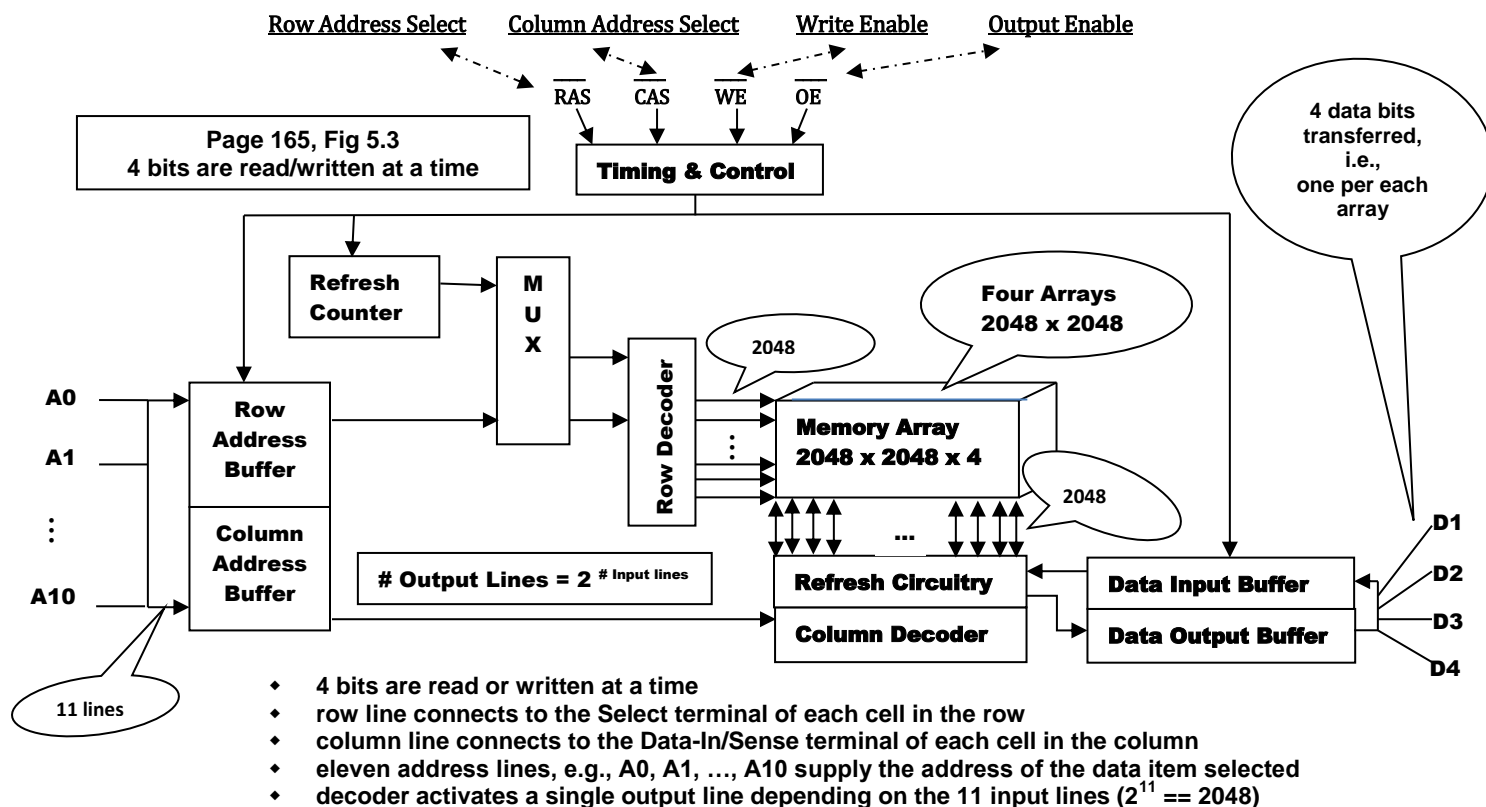
## Write-Mostly Memory

- EPROM – erasable programmable ROM <http://en.wikipedia.org/wiki/EPROM>
  - optical media
  - all storage cells on the chip are erased to an initial state by exposure to an intense ultra-violet light
  - erasure may be done repeatedly
  - erasure may take 10-20 minutes to perform
  - one transistor per cell
  - more expensive than PROM
- EEPROM – electronically erasable programmable ROM <http://en.wikipedia.org/wiki/EEPROM>
  - rewritable at the byte level without prior erasure
  - writable in place, i.e., on-line, using ordinary bus control, address & data lines
  - field-effect transistors [http://en.wikipedia.org/wiki/Field effect transistor](http://en.wikipedia.org/wiki/Field_effect_transistor)
  - write operation takes several hundred microseconds per byte, i.e.,  $\approx 0.5 - 0.01$  milliseconds
  - completion time: read operation  $\ll$  write operation
  - more expensive than EPROM
  - less dense than EPROM
- Flash Memory
  - rewritable at the block level without prior erasure
  - one transistor per cell
  - entire blocks of memory cells are erased in a single *flash*
  - erasure of entire flash memory can be accomplished in a few seconds

Flash memory is not byte addressable

## Chip Organization & Functional Logic

- Organizational Principle -- number of bits of data read/written at a time
  - Physical arrangement of cells in the array is the same as the logical arrangement of words in memory, i.e., array contains W words of B bits each, e.g., 16-Mbit chip organized as 1M of 16 bit words
  - One bit per chip arrangement, data is written 1 bit at a time



- ❖ Using DRAM 2048 x 2048 x 4 Memory Array architecture → multiple DRAMs must be connected to a memory controller in order to hold a word of data, e.g., two DRAMs are required to transfer one byte of data
- ❖ A0, A1, ..., A10 are used to pass both row & column address information
  - A0, A1, ..., A10 are used to pass row address information with the Row Address Select line as well as either the Write Enable line or the Output Enable line set
  - A0, A1, ..., A10 are used to pass column address information with the Column Address Select line as well as either the Write Enable line or the Output Enable line set
- ❖ Using one more address line, e.g., A0, A1, ..., A10, A11 doubles the number of rows and columns thus quadrupling the amount of memory on an array, i.e., output rows  $2^{12} = 4096$  and output columns  $2^{12} = 4096$  yields an array 4096 x 4096 x 4  
 Note: 4096 x 4096 x 4 → 67,108,864 whereas 2048 x 2048 x 4 → 16,777,216  
 16,777,216 x 4 → 67,108,864
- ❖ Refresh Circuitry
  - disable DRAM chip
  - the refresh counter selects the row values one at a time; the selected values are supplied to the row decoder and the Row Address Select line is activated. The data is read out and rewritten into the same location thus each cell in the row is refreshed.

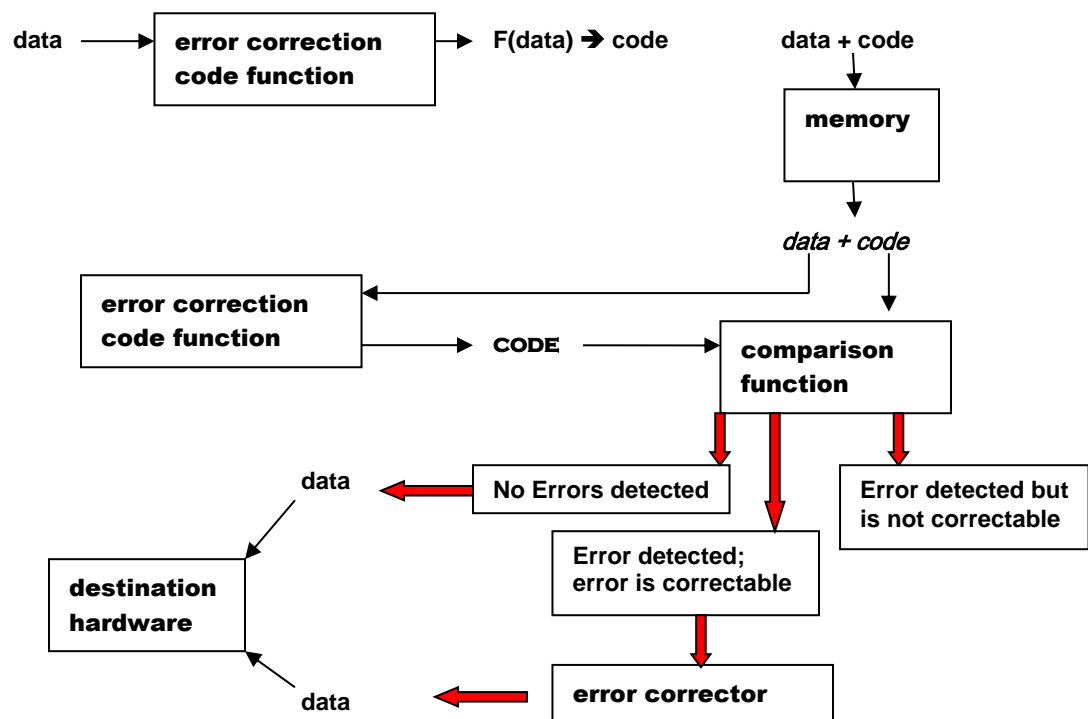
- **Chip Packaging**
  - EPROM chip pg 166 fig 5.4    8 Mbit chip    organized as 1M x 8 one word/chip package
  - DRAM chip pg 167 fig 5.5    16 Mbit chip    organized as 4M x 4  
4 arrays 2048 x 2048  
 $2^{11} \times 2^{11} \rightarrow 2^{22} \rightarrow 4M$   
NC pin ("no connect" provided to provide even number of pins)

#### Module Organization

- RAM chip contains 1 bit per word  $\rightarrow$  n RAM chips required for n bit word,  
e.g., 8 RAM chips required for byte addressable memory
- other configurations become more complex
- interleaved memory
  - main memory composed of a collection of DRAM chips
  - chips are grouped into **memory banks**
  - each bank may independently service a memory request; i.e.,
  - system composed of K banks can simultaneously service K requests
  - consecutive words stored in different banks  $\rightarrow$  transfer times for memory blocks will be increased

#### Error Correction

- **Hard Failure** – permanent physical defect in the cell
- **Soft Failure** – random, nondestructive event, alters content without damaging the cell
  - power supply fluctuations
  - alpha particles – radioactive decay
- procedure



#### Hamming Code

<to be discussed later>

## SDRAM (Synchronous DRAM)

- SDRAM moves data under the control of the system clock, i.e., synchronous access

### DRAM operation

- CPU sends addresses & control information to DRAM
- During access time delay, DRAM activates the high capacitance of the row & column lines, senses the data and routes the data to output buffers
- CPU must wait during the access time delay

see page 175 figure 5.12  
for internal logic diagram

see page 176 figure 5.13  
for timing chart activity

- **Processor**, or surrogate, issues instructions and address information which is latched by the SDRAM
- **SDRAM responds after a specified number of clock cycles**
- CPU can engage in other tasks while the SDRAM responds to the request
- SDRAM provides a mechanism to enable customization of chip operation to meet specific needs of system builders
- SDRAM performs best when transferring large blocks of data, e.g., multimedia, spreadsheets, word processing

## DDR-SDRAM (Double Data Rate SDRAM)

[http://en.wikipedia.org/wiki/DDR\\_SDRAM](http://en.wikipedia.org/wiki/DDR_SDRAM)

- Sends data to the processor twice per clock cycle – one on the leading edge, another on the following edge

## DDR2-SDRAM [http://en.wikipedia.org/wiki/DDR2\\_SDRAM](http://en.wikipedia.org/wiki/DDR2_SDRAM)

## DDR3-SDRAM [http://en.wikipedia.org/wiki/DDR3\\_SDRAM](http://en.wikipedia.org/wiki/DDR3_SDRAM)

## RDRAM (Rambus DRAM)

[http://en.wikipedia.org/wiki/Rambus\\_DRAM](http://en.wikipedia.org/wiki/Rambus_DRAM)

- special RDRAM bus asynchronous block-oriented protocol
  - defines impedances, clocking, signals very precisely
  - receives memory requests over a high-speed bus
  - request contains address, type of operation (read/write) and number of bytes desired
- RDRAM bus connects to the controller at one end and is terminated at the other end
- Clock signal originates at the terminated end, propagates to the controller end and is then reflected back to the terminated end
- bits are sent at both the leading and the following edge of each clock signal going toward the controller
  - signal rate 800 Mbps (cycling twice the clock rate)
- RDRAM module sends data to the controller synchronously to the master on the forward direction
- Controller send data to the RDRAM synchronously with the clock signal in the opposite direction
- initial 480 nanosec access time, it produces a 1.6 GBps data rate

Intel  
Pentium & Itanium processors

standard usage is send bits only at  
one of the edges of a clock signal

## CD-DRAM Integration of a small SRAM cache (16 Bb) onto a generic DRAM chip

- used as cache memory
- used as a buffer to support serial access of a block of data

[Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers \(Embedded Technology\)](#) by [Tammy Noergaard](#) (Feb 24, 2005)

Flash Memory Bez, R. et. al. Introduction To Flash Memory Proceedings of the IEEE, April 2003