Motivation

- Exponential performance increase at a low cost
- However, for some application areas low power consumption is more important than performance:
  - Mobile communications
  - Mobile computing
  - Wireless Internet
  - Medical implants
  - Deep space applications
  - Battery life time

Designing for Low Power: Approaches

- Trading area/performance for power
  - Power can be reduced by decreasing the supply voltage and allowing the performance to degrade.
    - Trading performance for power
  - But these techniques incur an area penalty.
    - Trading area for power
**Designing for Low Power: Approaches**

- Avoiding waste
  - Avoiding waste
  - Clocking module when they are idle
  - Glitching
  - Using dedicated rather than programmable hardware
  - Reducing control overhead by using regular algorithms and architectures
  - Designing systems to meet performance requirements

- Exploiting locality
  - Global operations inherently consume a lot of power.
    - Data must be transferred from one part of the chip to another at the expense of switching large bus capacitances.
  - A design partitioned to exploit locality of reference can minimize the amount of expensive global communications employed in favor of much less costly local interconnect networks.

**Crusoe Family of Processors from Transmeta**

- Introduction
- Software: Code Morphing
- Hardware: VLIW core
- Performance
- Applications
The Idea – David Ditzel

- Champion of simple chip architecture.
- 1995
  - Chief Technical Officer of Sun MicroSystems Inc.’s Sparc Business.
  - Working on emulation of x86 software on Sparc Processors.

Early 1995 left Sun and worked on his own idea.
- Was not happy with the complexity of the architectures of recent times.
- Some new ideas mixed with some old ideas to build a simple and fast architecture capable of running x86 code.
- Software hardware hybrid.

The Company - Transmeta

- Ditzel and Colin Hunter choose the name Transmeta and the company was formed in Summer of 1995.
- Use of contacts in the industry to recruit top brains for the ideas.
- Design started in the living rooms of the founders homes.
- Now employs many people.
**Innovation**

- Transmeta Crusoe chip
  - x86 Emulation
  - Very Long Instruction Word (VLIW)
  - Code Morphing
  - Simple Architecture
  - LongRun Technology
  - Virtual Devices
  - Low Power

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**Introducing a Software Layer**

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**Software: Code Morphing**

- Performs **dynamic binary translation**.
  - Compiles instructions from one instruction set architecture (ISA) to another ISA.
Decoding and Scheduling

Conventional x86 superscalar processors fetch binary instructions and decode them into separate micro-operations. Then they are reordered by the hardware and executed in parallel.

Code morphing translates an entire group of x86 instructions at once and stores the translation in a translation cache for future reference.
Decoding and Scheduling

- The translation step introduces many opportunities.
  - Due to high repeat rates the translation cache is frequently used to reduce overhead.
  - Can use much more sophisticated scheduling algorithms.
  - Much lower power consumption because translation is all in software.
  - Can optimize generated code, and by 'learning' which parts are executed often, can change levels of optimization dynamically.

Instruction Set Emulation

- Emulation is traditionally slow because of the way different ISAs handle condition codes and exceptions.
- Crusoe uses specific registers to emulate setting of condition codes by the processor (.c suffix is used after the instruction to show that condition codes need to be set).
- Exceptions are handled by using shadow registers, and a procedure called "commit and rollback"
Translation Step 2

Optimization
Elimination of
atoms + extra
condition
code options.

Optimized Native VLIW code
Native VLIW code

Translation Step 3

Optimized Native VLIW code

Scheduled Native VLIW code

Software’s Edge

Molecules explicitly encode the instruction-level parallelism, hence they can be executed by a simple VLIW engine.

The hardware doesn’t need to perform complex instruction reordering.

Simplicity means fast and low-power design.

Processor upgrades are simplified.

Software layer means that software developers don’t have to recompile programs.

New hardware architecture only needs a new code morphing software from Transmeta.
Software’s Edge

- Code morphing software can be upgraded independently into flash ROM.
- Software layer helps debugging process.
  - There are different ways to perform the same function so software can be changed in debug process.
- Software layer increases performance.
  - Timing of critical paths are improved.
  - Optimization is applied to remove unnecessary instructions.
  - Software reordering can be done much better than hardware by looking at a bigger window of instructions and applying more complicated algorithms.

Several ISA

- Allows you to mix instruction sets with ease because they are all emulated by the software.

Hardware

Modern x86 CPU

Transmeta’s Crusoe

[Diagram of Modern x86 CPU and Transmeta’s Crusoe]
Chip Simplifications

- No Superscalar decode, grouping or issue logic.
- No register renaming or segmentation hardware.
- No floating point stack hardware.
- No front end memory management.
- Less interlock and bypassing logic.
**Hardware Specifications**

- 128 bit High performance VLIW engine
- 2 Integer units (ALU's)
- Floating point unit
- Memory unit
- Branch unit

![Image of hardware specifications]

**Code Morphing Hardware Support**

- Handling exceptions by shadowing.
- Commit and rollback.
- Gated Store Buffer.
- Aliasing Hardware.
- Protection for self modifying code.
- LongRun Technology.
Performance

- Originally designed for 32 bit conversions i.e. Unix (TM3120).
- However 16 bit windows instructions translated poorly so (TM5400)
  - The chip was redesigned to give better support to Windows 95 16-bit applications.
  - Larger caches were also included for improved Windows performance.
- Two chips - Two different applications.

Low Power Consumption

- Fewer Transistors (simpler hardware)
  - Virtual devices
- TM3120 Chip Voltage of 1.5V
- LongRun Power Management (TM5400 Dynamically adjustable frequency & voltage)

Implications

- Low Power consumption means low heat
- Low heat means no need for noisy power hungry fans or heat sinks
- Smaller lightweight computers possible
- Economy and extended battery life for mobile computers
## Processor Thermal Comparison

Intel Pentium III  
Crusoe TM5400 Processor

## Comparison of Watts per Hour

Applications:
- Portable and embedded systems.
- Runs a mobile Linux kernel.
- Capable of running Internet applications:
  - Web browsers.
  - E-mail applications.
  - Streaming video.
Application of the 5400

- Ultralite Laptops.
- Microsoft Windows compatible.
- Computer makers backing Transmeta include: IBM, Fujitsu, FIC, NEC, and Hitachi.

Mobile Internet Appliance

- Web pads, Notebooks, Smart Phones, PDAs.

Super Parallel Computing

- Code-morphing allows big jobs to be processed with a mixture of CPUs easily.
- Crusoe CPU’s can receive a block of code and dynamically re-compile it into their own ISA.
Future Plans

- Targeting the Desktop market.
- Faster Crusoe chips
  - speeds in excess of 1.4Ghz
  - cache sizes as high as 2MB