Fault Analysis on Distribution Feeders With Distributed Generators

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***Abstract*—This paper shows that the current an inverter interfaced distributed generator (IIDG) contributes to a fault varies considerably, due mainly to fast response of its controller. This paper proposes a method to extend the conventional fault analysis methods so that IIDG contribution can be estimated in the fault analysis. The proposed method gives rms profiles of the fault currents of interest (IIDG contribution and the fault currents the protective device will see). Test results, based on a prototype feeder, show that the proposed approach can estimate the fault current's contributions under both balanced and unbalanced fault conditions.**

***Index Terms*—Distributed generation, distribution system, fault analysis.**

I. Introduction

EMERGING distributed generation technologies make it more likely that more and more distributed generators (DGs) will be connected to the utility distribution feeders and supply power to the system in the near future. To facilitate the interconnection of DGs to a distribution system, standards are being developed [1], [2]. But an engineering analysis is usually needed to assess the impact of the DG on the operation of the system, especially for DGs that supply about 10% or more of the feeder load [3]–[6].

One of the major impacts of a DG on a feeder will be during the fault conditions, as the DGs will contribute to the fault current. The fault contribution from DGs may have a major impact on the protection of the feeder [3]–[9]. As it is pointed out in [6], the fault contribution from a single small DG unit may not be large; however, the aggregate contributions of many small units, or a few larger units, can alter the short-circuit levels enough to cause protective devices to malfunction. Higher fault currents will especially affect the Reclosers (RC) on the feeder. For example, extra fault current from an upstream DG may bring the fault current seen by the *RC* to a level higher than the RC's maximum interrupting current limit and thus expose the *RC* to mechanical and thermal stresses that are beyond its limits. Extra fault currents from DGs will also impact the fuse operation, as they will cause the fuses to clear sooner than designed. This may cause Recloser-fuse miscoordination and thus impact the feeder's reliability considerably [6]–[8].

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To address these issues properly, we need fault analysis methods that can estimate the contribution of DGs to fault currents. Hence, relatively accurate short-circuit models for different types of DGs are needed in order to assess DG fault contribution during both the subtransient (first cycle) and transient (3–10 cycles) periods.

This paper proposes a method to extend the conventional fault analysis methods so that the new DGs can be included in the analysis, as the conventional analysis methods [10] do not include models especially for the new inverter interfaced DGs (IIDGs). Extending the conventional fault analysis to include the IIDGs is challenging, because, as it will be shown, it will require more detailed models than the models used to represent conventional turbine driven ac generators [6], [11]. In the next section, the behavior of the IIDG during fault conditions will be investigated, and the proposed approach will be presented. Test results are given in Section III.

II. Fault Analysis on Distribution Feeders

For conventional distribution feeders, the substation is the only source of power, and since the substations are usually away from big generation units, the fault current transients do not have the initial high "subtransient component" that one can see in a fault current of the transmission system. Therefore, the fault current is usually approximated by its steady-state value. Thus, the feeder can be represented by a steady-state model, in which the substation is represented by a Thevenin equivalent (i.e., a voltage source behind the source impedance), and the lines are represented by their series impedances. The loads are usually neglected, but if needed, loads can be represented by their equivalent impedances. The corresponding equivalent circuit can then be analyzed by using the nodal equations

$$[Y_f]\, V_f = I_{inj} \tag{1}$$

where Y_f is the node admittance matrix, V_f is the voltage at each node, and I_{inj} is the current injected at each node. This model can be for equivalent single phase or can be extended for three-phase analysis especially to include the mutual coupling effects [12], [13].

If there are conventional generators on the feeder, the above feeder model can be extended easily by using the simple Thevenin equivalent models for the generators [12]. For inverter interfaced DGs, the same technique cannot be applied, since as it will be illustrated below, the inverter alters the generator response considerably. Therefore, a new approach is needed in order to incorporate IIDGs into the fault analysis.

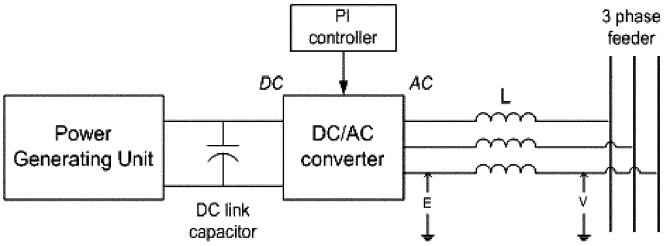


Fig. 1. Main components of an IIDG.

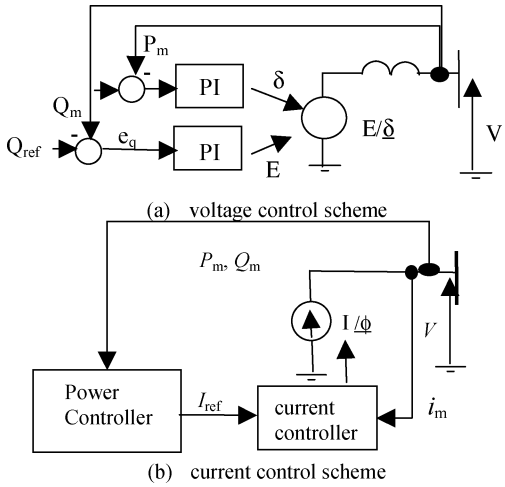


Fig. 2. IIDG representation for fault analysis under two control schemes.

A. DG Representation

Fig. 1 shows the main components of an IIDG. The power generating unit (PGU) produces the dc power and could be a fuel cell, micro turbine, or a photovoltaic. The dc voltage is then converted via an inverter to three-phase ac voltage. The controller on the inverter regulates the inverter active and reactive power output around the desired set point.

Due to the dc link capacitor between the PGU and the converter, the dc output voltage will remain almost constant during short transients, and therefore, we can assume a constant dc input voltage for the converter. Hence, during a transient, the IIDG response depends mainly on the inverter controller. There are mainly two control schemes used in practice.

In the voltage control-based scheme, the controller helps the inverter to synthesize a three-phase balanced ac voltage at the inverter terminals (with some harmonics that can be neglected for control purposes). To regulate the real and reactive power output of the IIDG, the controller adjusts the amplitude and the phase of this synthesized inverter voltage (E) with respect to its terminal voltage (V). Therefore, the voltage controlled equivalent circuit, shown in Fig. 2(a), can be used to represent the IIDG during the transient period for this control scheme [15], [16]. As the figure indicates, in practice, a simple PI-type controller is used for regulating the power output of the DG.

The main disadvantage of this scheme, as it will be illustrated later on, is that the current cannot be directly controlled. Hence, the newer controllers may use a current control scheme. This control scheme, as Fig. 2(b) illustrates, uses two loops; the inner loop controls the current output of the DG and the outer loop regulates the power output [15]. The outer power controller acts like a supervisory controller and determines the current reference ($I_{\rm ref}$) for the fast inner current controller.

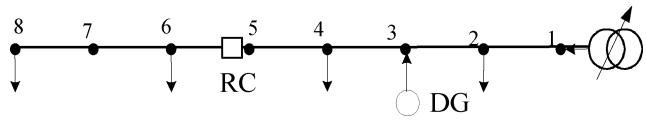


Fig. 3. Prototype feeder.

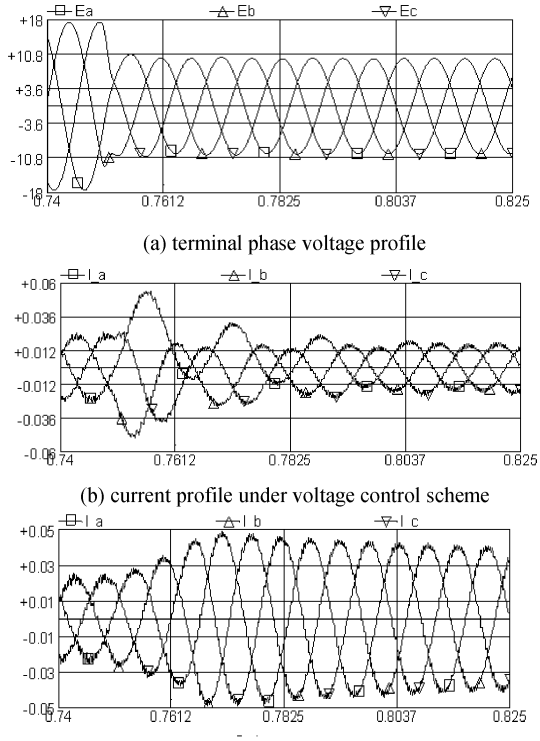


Fig. 4. IIDG response to a remote fault under two different control schemes (fault is at t = 0.75 s, time in s, currents in kA, and voltage in kV).

To illustrate the response of an IIDG to a fault, we simulated a case that corresponds to an IIDG connected upstream of a *RC* on a feeder, which is illustrated in Fig. 3 and described later in the test results section. In this case, we are interested in the contribution of the DG to the fault current the *RC* will see. Fig. 4 shows the DG current and voltage waveforms for a fault at the end of the feeder when DG operates under the two different control schemes.

Fig. 4 shows that under the voltage control scheme, the initial current overshoot is high and then controller brings the current to a steady state rather quickly, within a few cycles. Under the current control scheme, the current increases much slower and then decreases back to the steady-state value rather slowly. The slow corrective response under current control is mainly due to the slow response of the outer power control loop. However, the current is much controlled under this scheme. The current contribution under current control can be even more limited for solar applications where the outer power control loop is not used or is very slow [2].

Note that this prototype scenario corresponds to the IIDG fault contribution for a remote fault, and thus the contribution of fault current is within the maximum current rating of the converter, which is typically twice the normal rating. For close

faults, the IIDG is usually equipped with a protection scheme that turns the converter off when the current reaches the maximum limit [14]. Thus, this fault limiting needs to be considered as part of the fault analysis.

The figure also illustrates that the fault contribution of an IIDG will be higher especially during the transient period (first 5–10 cycles) if the IIDG is under voltage control scheme than under current control scheme. Therefore, in this paper the focus will be on the IIDGs with voltage control schemes. However, the method proposed here can be also adopted for the current controlled case.

B. Extending Fault Analysis to Include IIDG

Fig. 4(b) shows the initial current transients of the voltage controlled IIDG during the first few cycles of the fault. Since the current varies considerably during this period, DG needs to be represented in enough detail so that the controller's response can be taken into account and the peak current can be captured. Estimating the peak current is important as it determines the maximum stress levels a protection device has to be able to withstand [10]; also it is needed to estimate whether the fault current will be high enough for the IIDG protection to trip the IIDG off. Furthermore, if the IIDG stays online and feeds the fault, then we need to estimate its contribution to the fault current the downstream devices will see and interrupt during the transient period of first 5–10 cycles.

From the current and voltage profiles in Fig. 4(b), we distinguish the two transient periods, the subtransient of the first cycle during witch the current peaks, and then the next 5–10 cycles of transient period. The goal in the proposed approach is to consider the IIDG dynamics during these two periods and capture the current transients.

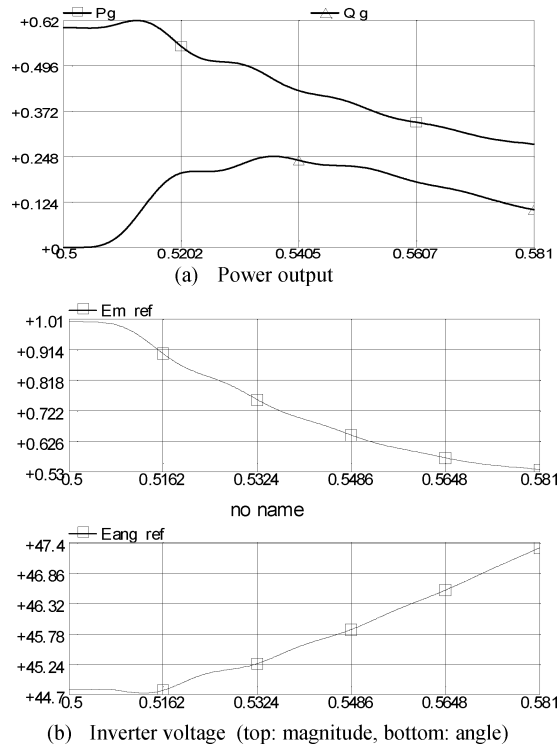
Subtransient Peak Current: Fig. 4(a) shows that the fault causes the voltage on the feeder to drop considerably in a very short time—within the first cycle—and stays almost flat. The voltage drop causes the current from DG to increase, and then the current is reduced by the controller action. These observations indicate that the peak current can be estimated by using conventional fault analysis, i.e., by the steady-state feeder model, as the voltage profile is flat. All we need is an estimate of the inverter internal voltage E.

To estimate the inverter voltage, let us look at the controller response. The power profile, shown in Fig. 5(a), illustrates that the DG power output does not chance as fast as the current during this period (in the figure, the power is almost flat during the first 8 ms after the fault at 0.5 s), mainly because the power measured is the average power. As a result, the controller does not change the inverter voltage much during the first half cycle, as Fig. 5(b) illustrates. Hence, a good approximation for the inverter is to assume that its voltage remains constant during this initial half cycle period at which the current peaks.

Therefore, the peak current of IIDG can be calculated as follows.

• *Calculate the prefault inverter internal voltage*

$$E_f^0 = \mathrm{V}_g^0 + \mathrm{jX}_\ell {}^* \mathrm{I}_g^{\mathrm{o}}$$



(a) Power output

(b) Inverter voltage (top: magnitude, bottom: angle)

Fig. 5. IIDG power and inverter voltage profiles during the first cycle.

where X_ℓ is the total link reactance (inverter output filer reactance plus transformer reactance) and I_g is the prefault current (that can be calculated using rated power).

• Represent each IIDG as a constant E_f behind its X_ℓ in the fault analysis, and perform a fault analysis on the feeder, i.e., use **(1)** to solve for the node voltages V_f.

• Calculate the branch currents the protection devices will see by using V_f.

• Calculate the peak current contribution from each IIDG

$$I_g^p = \frac{|E_f^0 - V_{gf}|}{X_\ell}$$

where V_{gf} is the IIDG bus voltage calculated in the previous step.

• If $I_g^p > 2I_g^0$, then IIDG most likely will trip even before the current reaches its peak.

Note that the main assumption made in the above discussion is that the voltage drop following the fault is fast and does not have any appreciable subtransient component. This is usually the case in practice, as pointed out earlier. But a good check for this is the Thevenin impedance, as seen by the source voltage at the substation during the fault. This impedance indicates how fast the transient component of the current and voltage waveforms will decay. For the transient component to reduce consid-

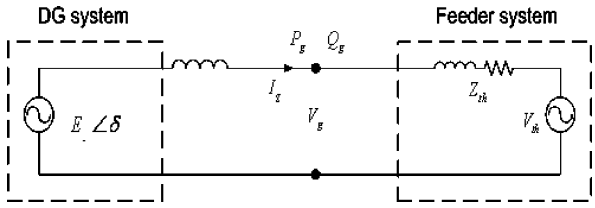


Fig. 6. DG and feeder as two coupled systems.

erably during the first half cycle, time constant determined by the Thevenin impedance should be less than 8 ms, i.e.,

$$\tau_f = \frac{L_{\rm th}}{R_{\rm th}} < 8 \text{ ms}$$

where $X_{\rm th} = \omega^* L_{\rm th}$ and $R_{\rm th}$ are the Thevenin impedance components. This condition is usually satisfied, as the feeder branches have small X/R ratios. For the prototype system, the calculated time constant is about 1.7 ms.

Transient Current: If a DG has not exceeded its peak current limit during the first cycle, then it will feed the fault during the transient period. As Fig. 4(b) illustrates, the current profile decreases after the initial peak due to the controller action. To capture the current profile, we need to capture the dynamic interactions between the feeder and the IIDG. For this, the feeder and the DG can be represented as two coupled systems shown in Fig. 6. Each system can be represented by its own dynamic set of equations and the interactions occur via the coupling variables as follows:

$$\textbf{Feeder:} \quad \dot{X}_s = f_s(X_s, E_f) \tag{2}$$

where

E_f equals (E, δ);

X_s state variables for the feeder.

$$\textbf{DG:} \quad \dot{E}_f = f_g(E_f, U_g) \tag{3}$$

where

U_g = (P_g, Q_g).

As these equations indicate, the inverter voltage E_f determines the interactions between the two subsystems. Hence, if we approximate the coupling variable E_f as constant (provided that we choose a simulation step length small enough so that E_f does not change much), then we can solve the two subsystems sequentially, as follows.

For each time step t_k:

A) *Feeder response update*

- Given the DG internal voltage E_f^k, approximate it as constant during the time step, and use **(2)** to update the feeder variables and obtain X_s^{k+1}, which contain the node voltages V^{k+1} and the branch currents the protection devices will see, such as the recloser current I_{rc}^{k+1}.
- Use the new DG terminal voltage V_g^{k+1} to update the DG power output $U_g^{k+1} = (P_g^{k+1}, Q_g^{k+1})$ using the DG equivalent circuit in **Fig. 6**.

B) *DG response update*

- Given U_g^{k+1}, assume that U_g varies linearly from U_g^k to U_g^{k+1} during $t_k - t_{k+1}$, and update the inverter voltage E_f^{k+1} using DG controller model in **Fig. 2(a)**.

These updates will be elaborated below. Another issue that will be addressed below is the selection of the time step, as it would impact the constant inverter voltage assumption we have in the feeder update in step A.

a) Feeder Response Update: In the feeder update step, the inverter voltages of the IIDGs are given, and we need to estimate the new feeder state X_s^{k+1}, which are the node voltages. This can be achieved as follows.

First, since we approximate E_f of the DG as constant during a time step, we can calculate what the corresponding steady-state values would be for the feeder using (1), i.e.,

$$[Y_f]V_f(ss) = I_{inj}(E_f). \tag{4}$$

Using the new node voltages, we then can calculate the corresponding steady-state current and power output of the DG as follows:

$$\begin{aligned} I_{gss}^{k+1} &= \frac{(E_f^k - V_{gss}^{k+1})}{jX_l} \\ P_{gss}^{k+1} + jQ_{gss}^{k+1} &= V_{gss}^{k+1}(I_{gss}^{k+1})^*. \end{aligned} \tag{5}$$

The next step is to determine how these variables vary during the time step. For this, we simulated the assumed conditions using EMTDC. Fig. 7 shows how P_g, Q_g changes when we change E_f stepwise half cycle after the fault occurs. This figure illustrates that the P_g, Q_g change from the initial state to the new steady state in a well-defined, exponential fashion with the same time constant "τ_g." Therefore, the change in $u = (I_g, P_g, Q_g)$ can be approximated as follows:

$$u(t) = u^k + (u_{ss}^{k+1} - u^k)(1 - e^{-t/\tau_g}). \tag{6}$$

In another words, the feeder response can be approximated at the DG node by a first-order circuit, i.e., by the Thevenin equivalent of the feeder at the DG node. Indeed, if we calculate the Thevenin equivalent impedance $\rm Z_{th} = R_{th} + jX_{th}$ of the prototype feeder at the DG node using (1), and determine the corresponding time constant of the circuit $\tau_g = L_{\rm th}/R_{\rm th}$, we get $\tau_g = 34$ ms. (See details in the test results.) This value closely matches the time constants of the $\rm P_g$ and $\rm Q_g$ curves in Fig. 7. Note that the impedance seen by DG is during the fault, so $\rm Z_{th}$ should be calculated by including the fault impedance in (1).

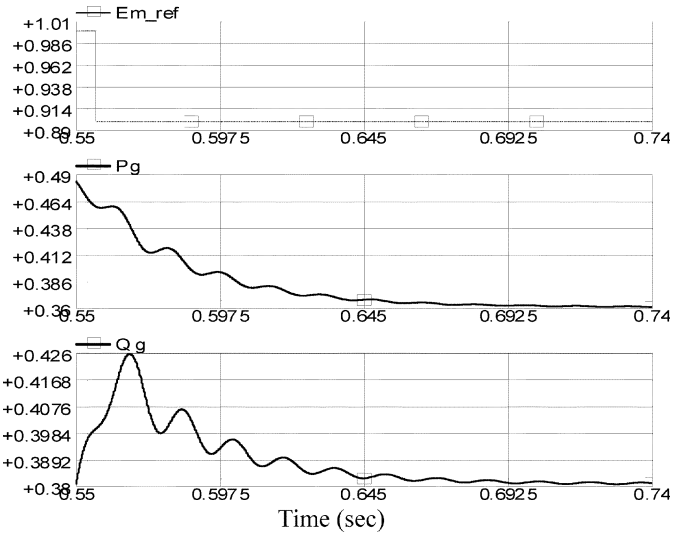


Fig. 7. Feeder response to a change in inverter voltage.

Finally, based on the above observation that the variation in u can be approximated by (6), the new $u^{k+1} = (I_g^{k+1}, P_g^{k+1}, Q_g^{k+1})$ can be estimated using (6), as

$$u^{k+1} = u(T) = u^k + (u_{ss}^{k+1} - u^k)(1 - e^{-T/\tau_g}). \quad (7)$$

b) DG Response Update: DG response is updated using the model in Fig. 2(a). Since the controller is usually of the PI type, it can be represented with a transfer function of the following form:

$$H_c = k_p + \frac{k_i}{s}. \quad (8)$$

For time-domain simulations, the controller can be discretized using the trapezoidal rule. The resulting discretized controller model then becomes

$$y^{k+1} = y^k + e^{k+1}\left[k_P + \frac{k_i T}{2}\right] + e^k\left[-k_P + \frac{k_i T}{2}\right] \quad (9)$$

where "e" and "y" are the controller input and output, respectively, and "T" is the time-step length. Hence, given the input to the two PI controllers, which are the active and reactive power errors

$$e_p = P_{\text{actual}} - P_{\text{set}}, \qquad e_q = Q_{\text{actual}} - Q_{\text{set}}.$$

The controller outputs $y = (E, \delta)$, can be determined using (9).

The controller parameters k_p and k_i are usually tuned to have a bandwidth f_{bw} of two orders of the line frequency [14]. Our simulations indicate that typical values for them are $k_p = 3$ and $k_i = f_{\text{bw}}$, respectively, as they provide the desired bandwidth and yield a good underdamped step response. Note that the gain constant k_p determines the initial response, and the time constant $T_i = 1/k_i$ determines the rate of correction. Hence, k_i is a more important parameter for estimating the transient current, and it is mainly determined by the controller bandwidth.

c) Time Step Selection: The goal in time-step selection is to choose the time step "T" such that the IIDG inverter voltage (E_f) does not change much during each time step, and thus, the approximation in the feeder update step will be acceptable. Note that the controller response to a fault will be rather slow as it will react to changes in real and reactive power output of the IIDG. Since the power measurements the DG uses are average values (over a cycle), the change in power is rather slow as Fig. 7 illustrates. As pointed out before, the rate of change of the power is mainly determined by the Thevenin impedance seen by the inverter τ_g. Hence, a good time step T can be selected based on this time constant as

$$T = \frac{3\,\tau_g}{10}$$

which corresponds to about 10% approximation error. For the prototype system, this corresponds to about 10 ms.

III. Test Results

To test the performance of the proposed fault analysis method, simulations have been performed on the IEEE 34-node prototype feeder [17], which represents a long feeder serving a mixed set of loads. The feeder is modified by adding a DG on the main feeder and an *RC* at the downstream of the DG, as Fig. 3 shows. The DG is modeled as fuel cell with a controller to regulate the DG's active power and power factor (DG model details are given in [16]). DG is assumed to be rated 750 kVA, 480 V, and connected to the feeder through a Δ-Y transformer with 3% reactance. The output filter of the converter is assumed to be 0.26 mH. To facilitate the simulations on EMTDC [18], the feeder section loads are lumped at the end of each section and represented by their equivalent impedances.

For the analysis, the feeder Thevenin equivalent impedance as seen by the DG is calculated first as part of the initial data needed for the fault analysis. The equivalent impedance for each phase is obtained by setting $E_f = 1$ p.u. and calculating the corresponding DG current using (1). This impedance of $Z_{\text{th}} = E_f/I_g = 20 + j270\,\Omega$ is then used to estimate the corresponding time constant as

$$\tau_g = \frac{\frac{X_{\text{th}}}{w}}{R_{\text{th}}} = \frac{\frac{270}{377}}{20} = 0.036 \text{ sec}.$$

Then the proposed procedure is used to estimate the fault current contribution of the DG and also the fault current seen by the RC during both the subtransient and the transient periods. Below are the results of the three different cases that have been investigated.

A. Case 1: Balanced Fault

In this case, the remote fault at the end of the feeder is assumed to be a three-phase balanced fault. A summary of the computation steps of the proposed method for this case is as follows.

Initial (Pre-Fault) Conditions:

- Given DG Power output: $P_g^0 = 600$ kW, $Q_g^0 = 0$,

do a power flow analysis and determine

$$V_g^0 = 0.97\angle -4.18 \text{ p.u.}; \quad I_g^o = 15\angle -4.18 \text{ A}.$$

- Calculate $E_f^0 = \mathrm{V}_g^0 + \mathrm{jX}_\ell * \mathrm{I}_g^o = 1.01\angle 44.8$.
- Set DG controller input to $e_p^0 = 0$, $e_q^0 = 0$.

Subtransient Peak Current:

• Given $E_f^0 = 1.01\ \angle 44.8$, use **(1)** to get the post-fault node voltages V_f.
• Calculate the peak currents for I_g and I_{rc} for the first cycle

$$I_g^p = \frac{|E_f^0 - V_{gf}|}{X_\ell} = 26.8 \text{ A}$$
$$I_{rc}^p = \left|\frac{\Delta V_{bf}}{z_b}\right| = 163.5 \text{ A}$$

where $\Delta V_b = V_4 - V_5$ is the voltage drop across the branch on which *RC* is located and Z_b is the corresponding branch impedance.

Transient Period: time step $\mathrm{t}_1 = \mathrm{T}\ (0.01\ \mathrm{s})$

a) Feeder Response:

• Let $E_f^1 = E_f(t_1) \cong E(t_0)$ (i.e., assume E_f remains constant during $t_0 - t_1$).
Use **(4)** to get the new steady-state node voltages $\boldsymbol{V}_{ss}^1$.
• Calculate corresponding DG and *RC* values using **(5)**, i.e.,

$$I_{gss}^1 = \frac{(E_f^1 - V_{gss}^1)}{jX_l} = 23 \text{ A}$$
$$P_{gss}^1 + jQ_{gss}^1 = V_{gss}^1 (I_{gss}^1)^* = 418(\mathrm{kW}) + \mathrm{j}501 \ (\mathrm{kVar})$$
$$I_{rcss}^1 = \left|\frac{\Delta \mathrm{V}_{\mathrm{bss}}^1}{\mathrm{z}_b}\right| = 161.7 \text{ A}.$$

• Use approximate update of **(7)** to estimate the DG and *RC* values at t_1

$$I_g^1 = I_g^0 + (I_{gss}^1 - I_g^0)(1 - e^{-T/\tau_g}) = 25.9$$
$$P_g^1 = 555, \quad Q_g^1 = 124$$
$$I_{rc}^1 = 163.1.$$

b) DG Response:

• Use P_g^1, Q_g^1 to calculate the controller input error

$$e_p^1 = 0.045 \qquad e_q^1 = -0.124.$$

• Use **(9)** to estimate the DG voltage E_f^1

$$E_f^1 = 0.918\angle 44.96.$$

Time Steps $t_2 - t_n$:
Repeat the computations of the first time step above.

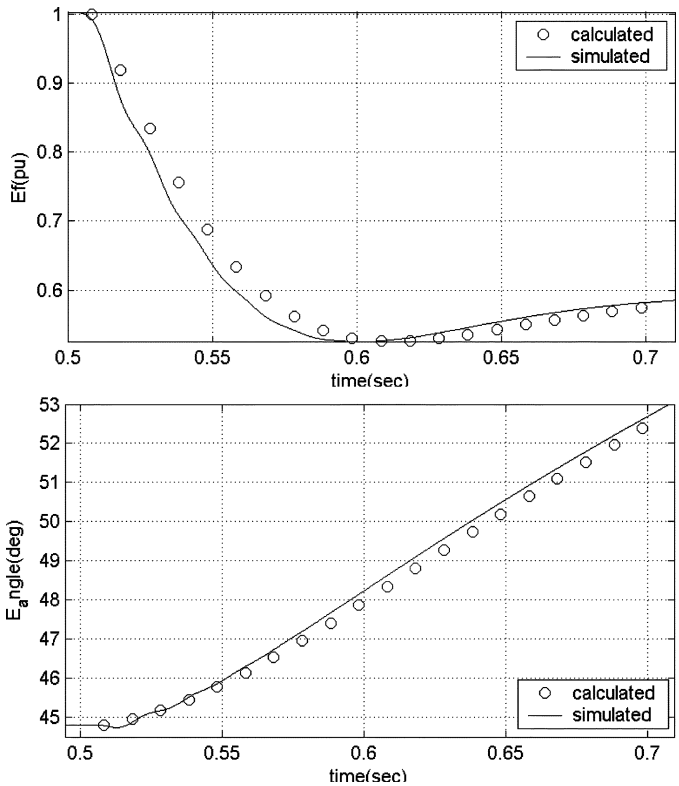


Fig. 8. IIDG inverter voltage—case 1.

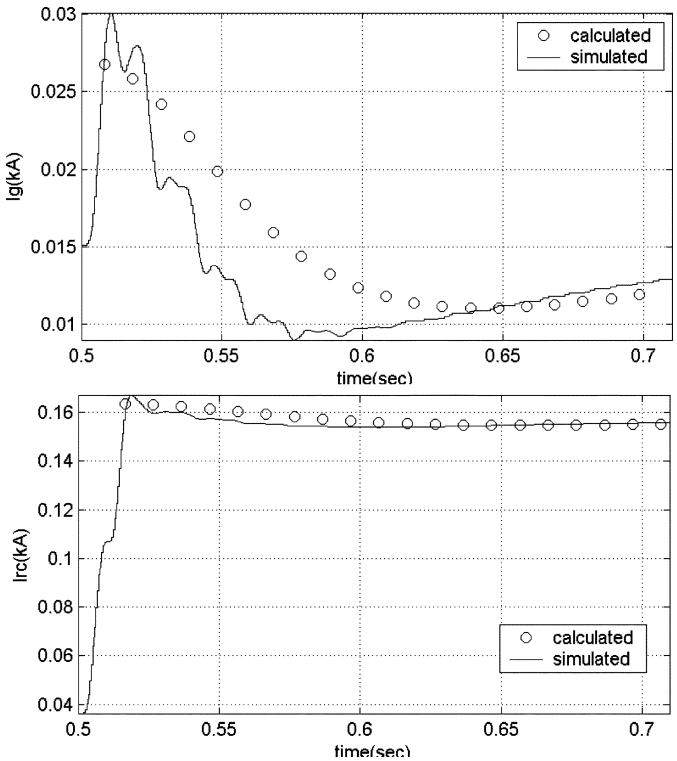


Fig. 9. RMS current profiles of IIDG and *RC*—case 1.

The results of this case are given in Figs. 8 and 9. Fig. 8 shows the DG inverter voltage obtained from the proposed method together with the one obtained from the EMTDC simulation. The figure shows that the calculated values follow the simu-

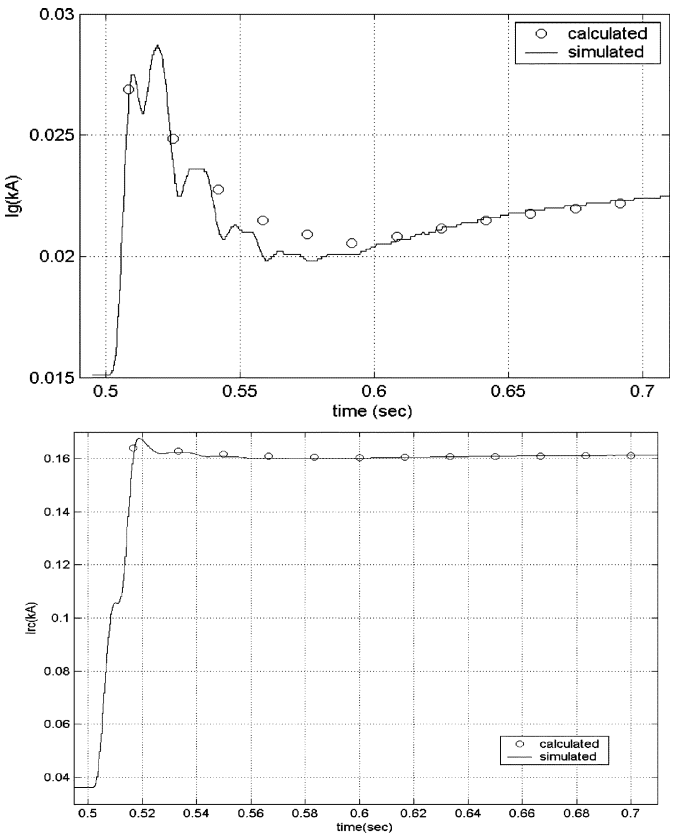


Fig. 10. RMS fault current profiles of DG and *RC*—case 2.

lated voltage profile very closely. Fig. 9 shows the comparison between the calculated and simulated fault currents for the DG and the *RC* and shows that the estimated fault currents track the simulated ones quite well. The peak RMS currents calculated for the *RC* and the DG are

$$I_g^p = 26.8\ \text{A} \qquad I_{rc}^p = 163.5\ \text{A}.$$

These estimates are close to the simulation-based values of 29 and 166 A, respectively. Note also that the calculated transient current profile for the DG current is smoother than the actual profile, and calculated values tracks the simulated values very close after about six cycles (100 ms). Since for remote faults, the *RC* will interrupt the faults after at least five cycles, the method will give very good estimate of DG and *RC* currents.

B. Case 2: Unbalanced Fault

In this case, the fault at the end of the feeder is assumed to be a phase-to-ground fault. The same analysis procedure has been repeated for this case, as the procedure can handle both balanced and unbalanced cases. Fig. 10 compares the estimated fault currents on the faulted phase for the DG and the *RC* with the simulation values. The figure shows again that the estimated fault currents closely follow the simulation values. Note that in this case, to test the sensitivity of time-step value, the time step has been increased to 16 ms, and the results indicate that results are not very sensitive to step-size selection.

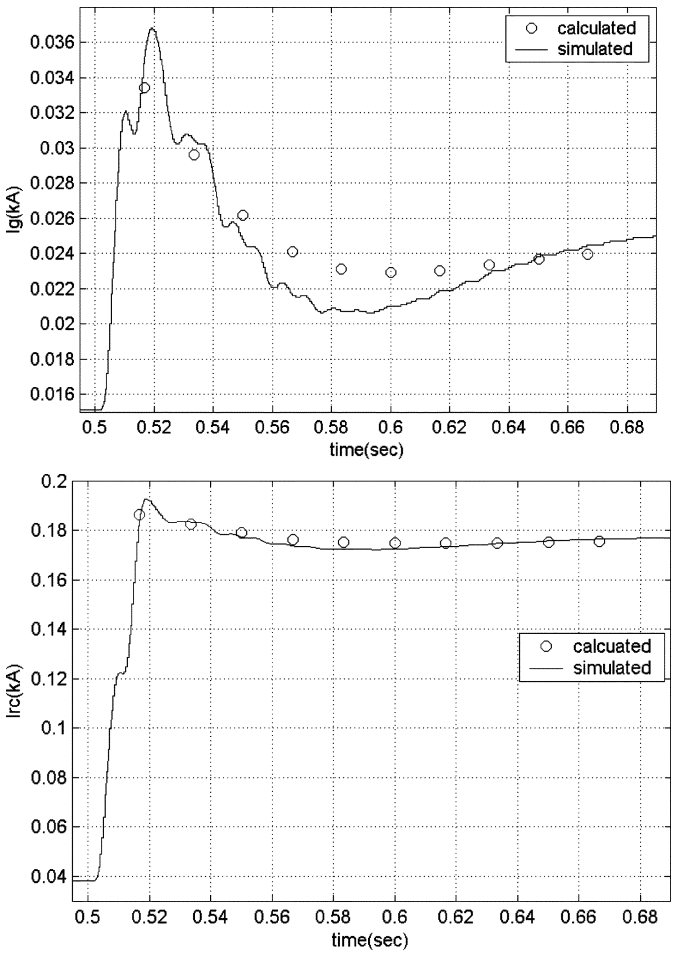


Fig. 11. RMS fault current profiles of IIDG and *RC*—case 3.

The first cycle peak RMS currents for IIDG and *RC* for this case are estimated as

$$I_g^p = 27\ \text{A} \qquad I_{rc}^p = 164\ \text{A}.$$

These values are close to the actual peak currents of 29 and 168 A, respectively. Fig. 10 shows that the tracking performance of the estimated current profile is about the same as in the balanced case.

C. Case 3: Two DGs

In this case, another IIDG has been added to the feeder at node 4 (see Fig. 4), which is downstream of the first IIDG and closer to the RC. The fault is again a phase-to-ground fault at the end of the feeder. Fig. 11 compares the estimated fault currents on the faulted phase for the second IIDG and the *RC* with the simulation values. The figure shows again that the estimated fault currents closely follow the simulation values.

The first cycle peak RMS currents for IIDG and *RC* for this case are estimated as

$$I_g^p = 33\ \text{A} \qquad I_{rc}^p = 186\ \text{A}.$$

These values are close to the actual peak currents of 36 and 192 amps, respectively. Fig. 11 shows that the performance of the proposed method for this case is about the same as that of the previous cases.

IV. Conclusions

This paper first shows that the fast response time of IIDGs make it necessary to consider their fault current contributions during the subtransient period as well as transient period. The paper then develops a method to capture IIDG behavior during a fault period. This model is then used to extend the conventional fault analysis method so that IIDGs can be represented in the analysis. The proposed method gives rms profiles of the fault currents of interest (IIDG contribution and fault currents at protective device locations) so that both the peak values as well as current transients during the transient period can be estimated. Test results, based on simulations on the prototype feeder, show that the proposed approach can accurately estimate fault currents under both balanced and unbalanced fault conditions.

The extra data the method needs for each DG are rather minimum: rating data, controller bandwidth and gain constants, and connecting transformer data.

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