1. Course Number and Name: ECE 527L – Application Specific Integrated Circuit Development Laboratory

2. Credit Units/Contact Hours: 1/3

3. Course Coordinator: Ronald W. Mehler

4. Text, References & Software

Recommended Text:
ECE 527L Laboratory Manual Laboratory and procedure handouts

Software
Cadence NC Verilog simulator, Synopsys Design Compiler, Synopsys PrimeTime Static Timing Analyzer, Synopsys Test Compiler

5. Specific Course Information

a. Course Description
This course is a companion to ECE 527, Application Specific Integrated Circuit Development. In the laboratory, students apply the lessons of ECE 527 to code circuits in Verilog HDL, synthesize them for varying performance goals and modify the implemented designs for testability. This is accomplished through use of state-of-the-art industrial design automation software. One three-hour lab per week.

b. Prerequisite by Topic
ECE 526. Students need a thorough understanding Verilog for digital integrated circuit description.

c. Elective Course

6. Specific Goals for the Course

a. Specific Outcomes of Instructions – After completing this course the students should be able to:
As a result of taking this course, the students should be able to synthesize digital circuit designs, analyze synthesis results, modify the designs to meet performance goals and test requirements and handle clock domain crossings to minimize the probability of metastability failures.
1. guard against metastability by properly synchronizing signals from different time domains
2. synthesize a netlist from a hierarchical set of Verilog circuit description files
3. modify a design for testability
4. create factory test vectors to ensure proper functioning of the fabricated circuits
5. perform static timing analysis on synthesized netlists
6. check for any design rule violations.

b. Relationship to Student Outcomes
This supports the achievement of the following student outcomes:

a. An ability to apply knowledge of mathematics, science, and engineering to the analysis of
electrical and computer engineering problems.

b. An ability to design and conduct scientific and engineering experiments, as well as to analyze and interpret data.

c. An ability to design systems which include hardware and/or software components within realistic constraints such as cost, manufacturability, safety and environmental concerns.

e. An ability to identify, formulate, and solve electrical and computer engineering problems.

g. An ability to communicate effectively through written reports and oral presentations.

k. An ability to use modern engineering techniques for analysis and design.

m. An ability to analyze and design complex devices and/or systems containing hardware and/or software components.

7. Topics Covered/Course Outline
Lab 1. Introduction to synthesis. Moving along the area/speed curve. Modify design for increased performance.
Lab 2. Hierarchical synthesis.
Lab 3. Adding boundary and logic scan.
Lab 4. Logic and memory BIST.
Lab 5. Design project—complete backend procedure from HDL to GDSII.

Prepared by:
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