Course Syllabus
ECE524 – FPGA/ASIC Design and Optimization Using VHDL
Department of Electrical & Computer Engineering

1. Course Number and Name: ECE 524 – FPGA/ASIC Design and Optimization Using VHDL

2. Credit Units/Contact Hours: 3/3

3. Course Coordinator: Ramin Roosta

4. Text, References & Software

Recommended Text:
Ramin Roosta, Shahnam Mirzaei lecture notes,”Xilinx and Actel FPGA architectures”, CSUN.

Additional References:
1. Volnei A. Pedroni, Circuit Design with VHDL, MIT Press, 2004
5. Kevin Skahill, VHDL for Programmable Logic, Addison-Wesley, 1997

Software:
Xilinx Foundation ISE, Modelsim, Actel Libero, Mentor Graphics Design tools

5. Specific Course Information

a. Course Description
This course covers top down design methodology for FPGA and ASIC using VHDL. Hardware Description Language, (VHDL) modeling, simulation and synthesis tools are utilized to elaborate the material covered throughout the course. Xilinx (the Virtex series) and Actel (the SX and AX series) FPGA architectures and design methodologies are studied. Several sample designs are targeted and tested for each FPGA technology. ASIC design flow and design optimization techniques are discussed. ASIC design flow, constraint file generation, and test benches are also studied with their applications to some designs samples. The use of FPGAs in space and military applications and their reliability issues are discussed.

b. Prerequisite by Topic
Students must know conventional techniques in designing digital logic circuits. They must be familiar with a programmable logic devices and their implementation. They are required to know how to use VHDL in design description and Maxplus II software in design simulation and verification (ECE420). Students required to be taking the lab with the lecture (ECE524L).

c. Elective Course

6. Specific Goals for the Course

a. Specific Outcomes of Instructions – After completing this course the students should be able to:
1. Ability to utilize the top-down design methodology in the design of highly complex digital devices such as FPGAs/ASICs.
2. Ability to use learn/use modern hardware/software design tools to develop modern digital systems.
3. Ability to design verification and test of integrated circuits chips.
4. Ability to design, implement and test different Field Programmable Gate Array (FPGA) architectures and their Applications to real life such as cell phones, PDAs, etc.
5. Ability to participate in team projects including design inspection and optimization.
6. Ability to understand the reliability issues of the highly complex devices in harsh military and space applications.

b. Relationship to Student Outcomes
This supports the achievement of the following student outcomes:

a. An ability to apply knowledge of math, science, and engineering to the analysis of electrical and computer engineering problems.
b. An ability to design and conduct scientific and engineering experiments, as well as to analyze and interpret data.
c. An ability to design systems which include hardware and/or software components within realistic constraints such as cost, manufacturability, safety and environmental concerns.
e. An ability to identify, formulate, and solve electrical and computer engineering problems.
g. An ability to communicate effectively through written reports and oral presentations.
k. An ability to use modern engineering techniques for analysis and design.
m. An ability to analyze and design complex devices and/or systems containing hardware and/or software components.

7. Topics Covered/Course Outline
1. Introduction to VHDL, CAD tools and design methodology
2. Design Units in VHDL
3. Timing and Simulation
4. Basic elements in VHDL
5. Behavioral Modeling
6. Structural Modeling
7. VHDL Synthesis techniques and recommendations
8. Advanced Concepts in VHDL
9. Xilinx FPGA Architecture
10. Actel Anti-fuse FPGA Architecture
11. Introduction to ASIC Design methodology
12. ASIC versus FPGA coding style
13. System on a Chip (SoC)
14. Design constraints and optimization techniques.
15. Military and space application of FPGAs and ASICs

Prepared by:
Ramin Roosta, Professor of Electrical and Computer Engineering, November 2011
Ali Amini, Professor of Electrical and Computer Engineering, March 2013